USC University of Southern California

EE 105: Introduction to Electrical Engineering

Lab 2.1

Diode and transistor I-V characteristics

Yasser Khan

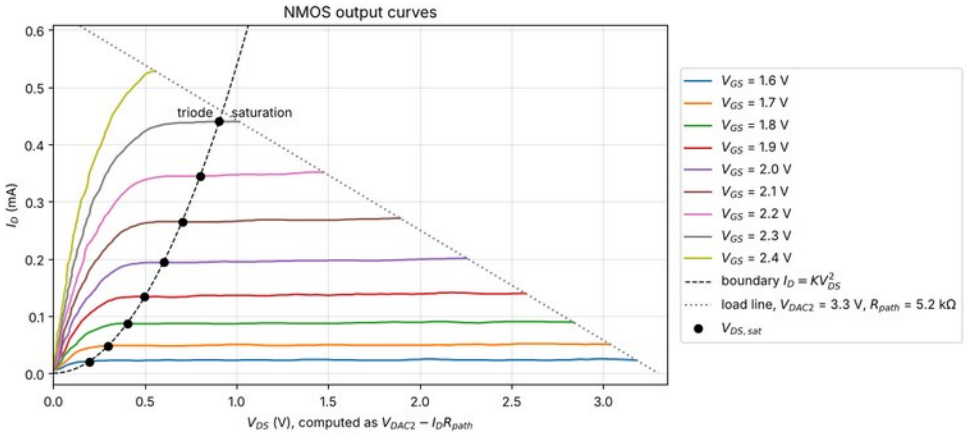
Rehan Kapadia

Today's mission

Sweep a diode and a MOSFET from Python and pull their key numbers out of the curves.

By the end of this lab you can:

- Measure a diode's **I-V curve** and its **knee voltage**
- Estimate the **ideality factor** n, with and without series resistance
- Measure a MOSFET's **transfer curve** and the resistance of its **drain path**
- Find **V_th** and **V_DS,sat** and mark triode and saturation



Output curves: triode, saturation, and the load line of the measured drain path.

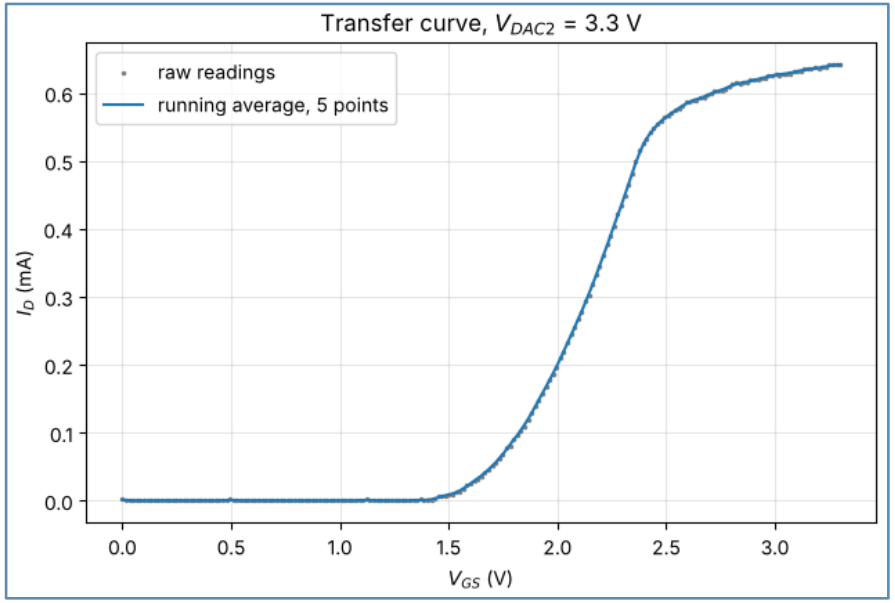
A Connect and find the parts — **10 min** → **B** The diode — **40 min** → **C** The MOSFET — **45 min**

Key takeaways

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What to remember from this lab, with the numbers that matter.

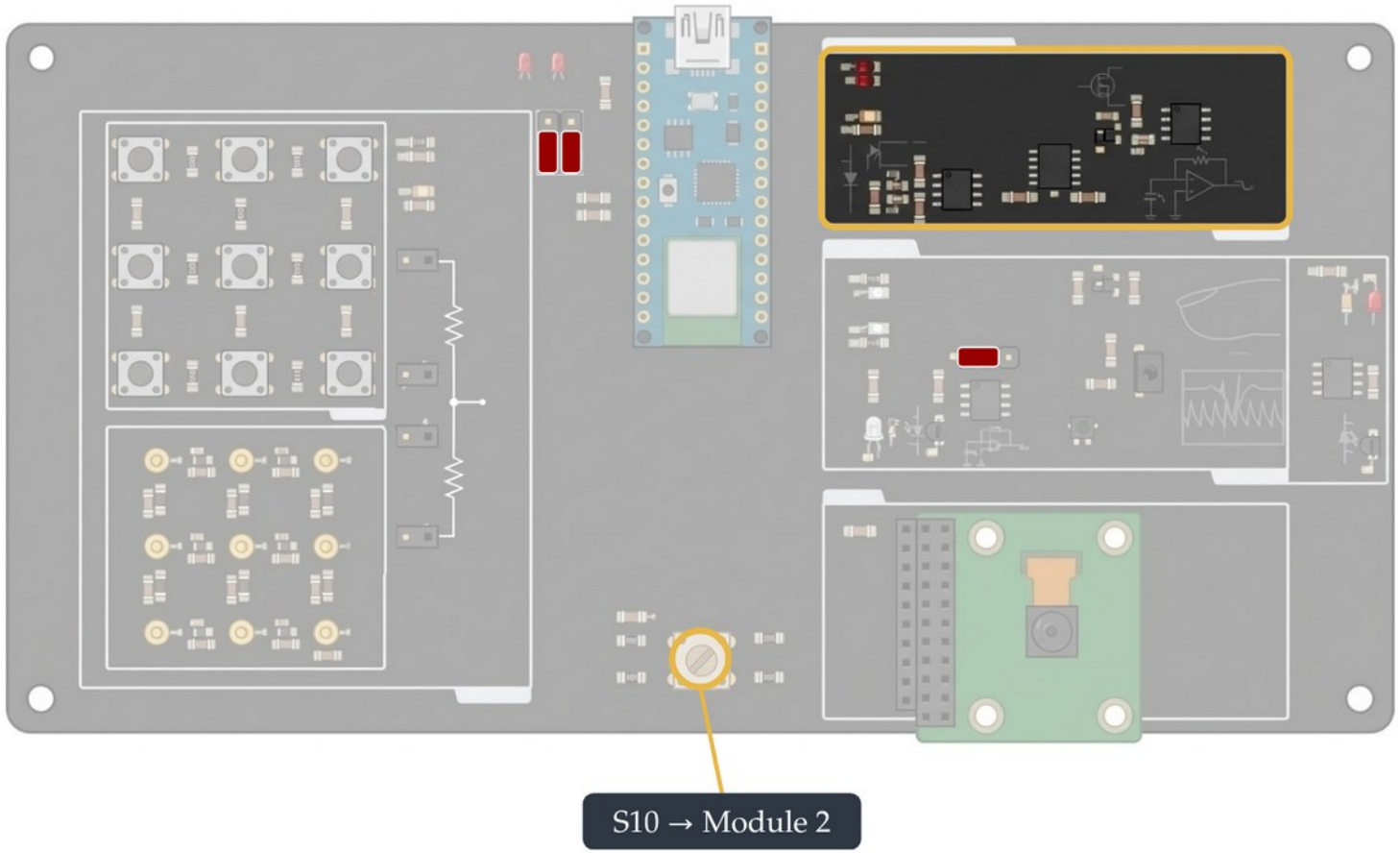
- **One ADC count is 3.2 µA** through the 1 kΩ sense resistor; a 5-point running average cuts the noise 2.2-fold
- **The diode reaches 0.5 mA at 0.61 V** and 2.5 mA at 0.74 V: a 0.7 V constant drop is within 3 % for 2 to 3.3 V
- **Two points give n ≈ 3,** because I·Rs (70 mV at 2.5 mA) is not junction voltage; the fit with Rs gives n = 1.93, Rs = 28 Ω
- **Measure the circuit, not the schematic.** The drain path is 5.3 kΩ, not 1 kΩ: I_D stops at 0.62 mA
- **√I_D is straight in V_GS while saturated.** Fit 0.05 mA to 0.6·I_max: V_th ≈ 1.4 V; curves saturate at V_GS - V_th



Expected result of C1 on the simulated board: the transfer curve flattens near 0.6 mA, the limit of the drain path.

SETUP

One selector turn: the devices block does everything through its DAC channels.



1. **S10 → Module 2**
   The devices block: diode, MOSFET and two difference amplifiers.

2. **Jumpers: no change**
   J7 and J8 caps stay on the Module 1 end.

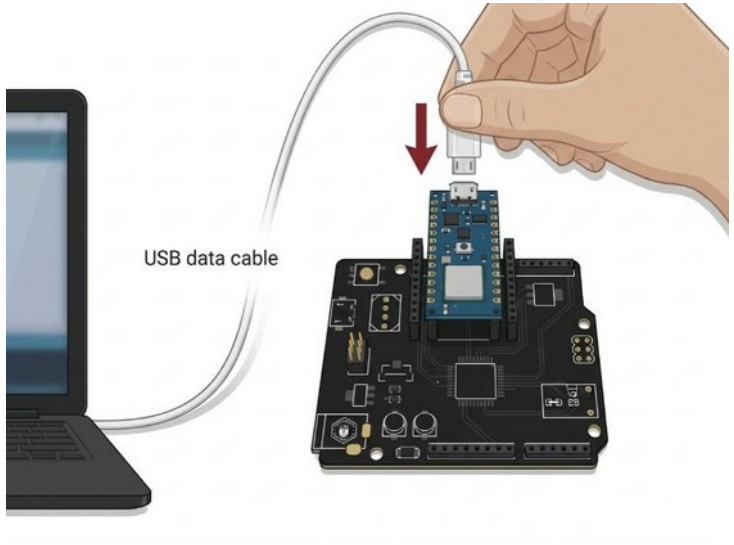
3. **Plugged in: nothing**
   The firmware drives the diode and the MOSFET itself.

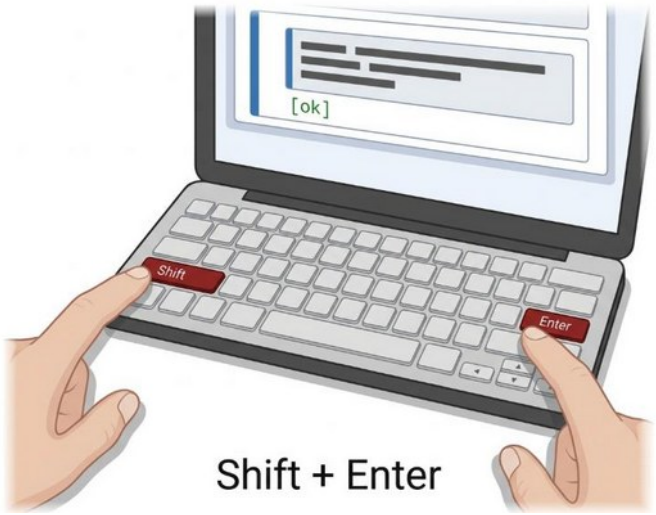
4. **USB data cable**
   Plug in after the selector is set.

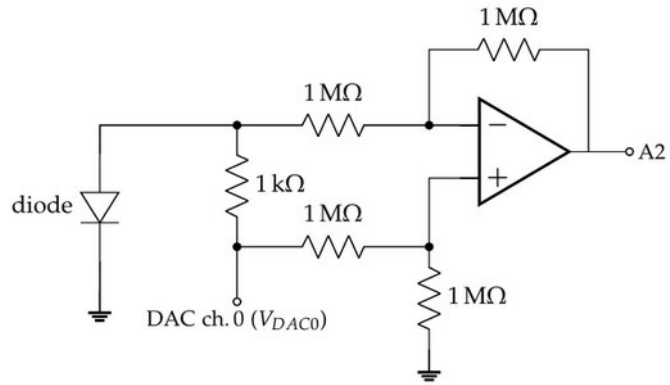
Part A: Connect

Plug in, run the first cell, then find the circuits on the board.

PART A **Goal: A1 · DO** connect; **A2 · RUN** constants; find the circuits.







1. Plug the USB data cable into the Nano
2. Run the first two cells with Shift+Enter
3. Find this circuit on the devices block

You should see: two **[ok]** lines, sense resistors 1 kΩ, one ADC count = 3.22 mV = **3.22 µA**, **16** readings per point and a **5-point** running average.

Check (Checkpoint 1): find the diode, the MOSFET, their 1 kΩ resistors, the gate pull-down and the TLV9102 op-amp.

Part B: Diode sweep and knee

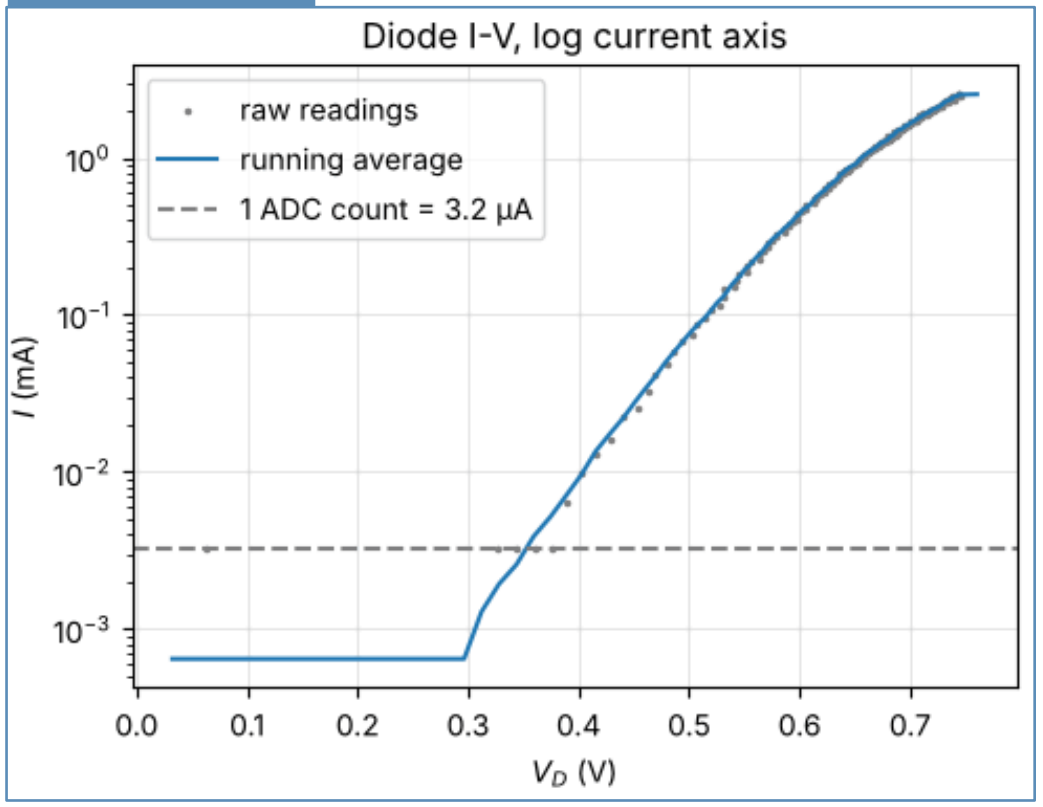
The DAC drives the diode through 1 kΩ: I = V_R / 1 kΩ and V_D = V_DAC - V_R.

PART B

Goal: sweep and smooth the diode, find its knee voltage and a first n.

- **B1 · RUN board.sweep**, 0 to 3.3 V in 16.5 mV: 201 points, a **5-point running average**, three plots
- **B2 · EDIT** Knee voltage: interpolate where I first reaches **0.5 mA**
- **B3 · EDIT** n from two points: 0.25 and 2.5 mA, then 10x lower

Expected result · B1



You should see: almost no current below about **0.5 V**; knee near **0.61 V**; about **2.5 mA** at V_DAC = 3.3 V; two-point n near **3**.

Part B: Series resistance and models

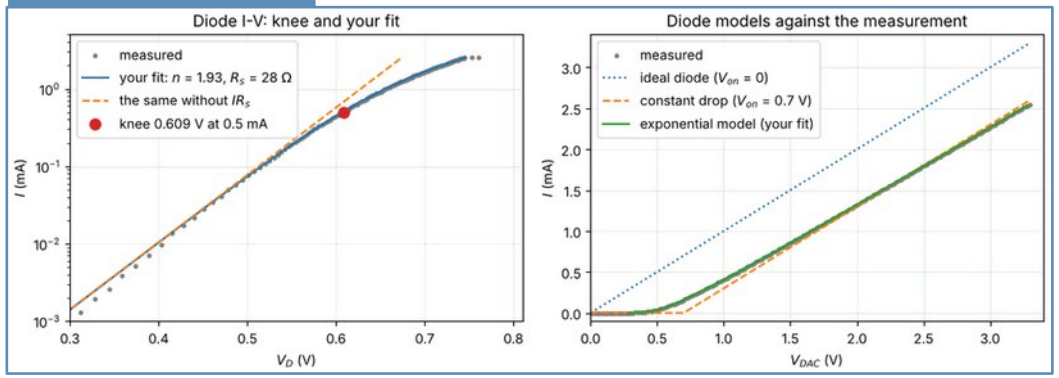
Two points give n near 3; a fit with series resistance brings it back between 1 and 2.

PART B

Goal: fit n and Rs, then compare the diode models.

- **B4 · EDIT curve_fit** with series resistance, from n = 2, I_S = 1 nA, Rs = 10 Ω
- **B5 · EDIT** The 0.7 V constant-drop model
- **B6 · RUN** Plots: your fit with and without I·Rs; the three models

Expected result · B6



You should see: two-point n near **3** (too high: part of V_D is I·Rs). The fit with Rs: **n between 1 and 2**, Rs **tens of ohms** (a real board's full sweep: 1.93 and 28 Ω).

Check (Checkpoint 2): the I-V plot shows the knee, and the fit with Rs gives n between 1 and 2.

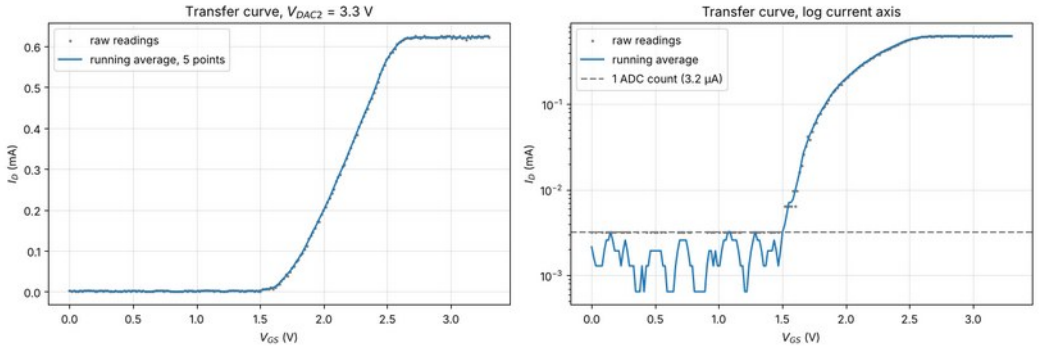
Part C: Transfer curve and drain path

I_D = V_A3 / 1 kΩ, but V_DS = V_DAC2 - I_D·R_path: measure the drain path first.

PART C

Goal: sweep the gate, find the current limit and R_path, then V_DS.

- **C1 · RUN board.transistor_transfer**: gate 0 to 3.3 V, smoothed and plotted
- **C2 · EDIT** Current limit I_max (V_GS ≥ 3.0 V) and **R_path = V_DAC2 / I_max**
- **C3 · EDIT id_vds(v_dac2, v_a3)**: V_DS = V_DAC2 - I_D·R_path



A real board: I_D levels off at 0.62 mA, the limit of its drain path.

You should see: I_max near **0.62 mA**, not 3.3 mA: R_path near **5.3 kΩ**, 4.3 kΩ more than the sense resistor.

Part C: Threshold and output curves

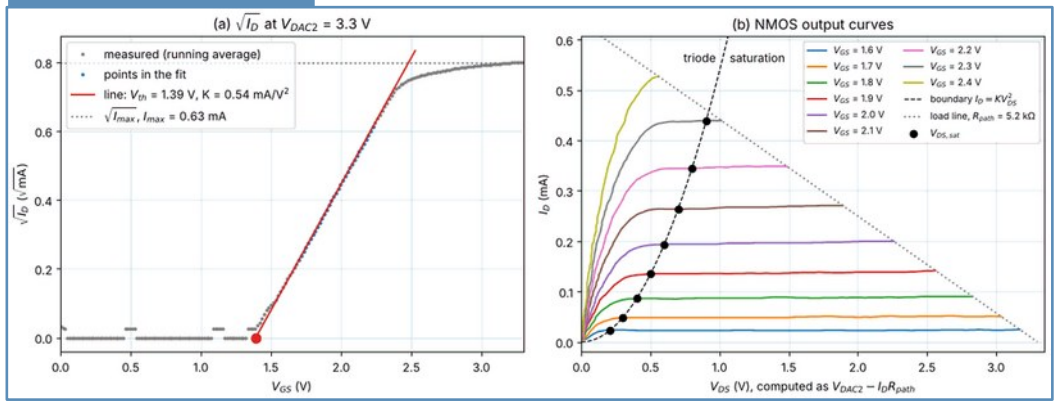
Fit only the rising part, then hold the gate and sweep the drain.

PART C

Goal: find V_th and K, measure the output curves and V_DS,sat.

- **C4 · EDIT** √I_D line, 0.05 mA to 0.6·I_max: V_th, K
- **C5 · RUN** V_GS = 1.6 to 2.4 V: one drain sweep per gate voltage
- **C6 · EDIT vds_sat**: crossing of $I_D = K V_{DS}^2$
- **C7 · RUN** √I_D with your line; curves against the **computed** V_DS

Expected result · C7



You should see: V_th near **1.42 V** (data sheet 1.0 to 2.0 V), K near **0.58 mA/V²**; V_DS,sat close to **V_GS - V_th**.

Check (Checkpoint 3): the output curves show both regions, and V_th is in the data sheet's range.

Stuck?

Check these first. If the fix does not help, raise your hand.

[!] Almost no current

S10 is not on Module 2. Turn it to the devices block and rerun the sweep.

I_D stops near 0.6 mA

That is the drain path, not the transistor: C2 measures R_path, C3 uses it.

curve_fit does not converge

Pass p0=p0 and the currents in amperes, not milliamperes.

V_th far below 1 V

Fit only 0.05 mA to 0.6·I_max (C4), not the flat top.

Few output curves rise

Shift VGS_STEPS (C5) so the top step gives about 0.9·I_max.

V_DS looks wrong

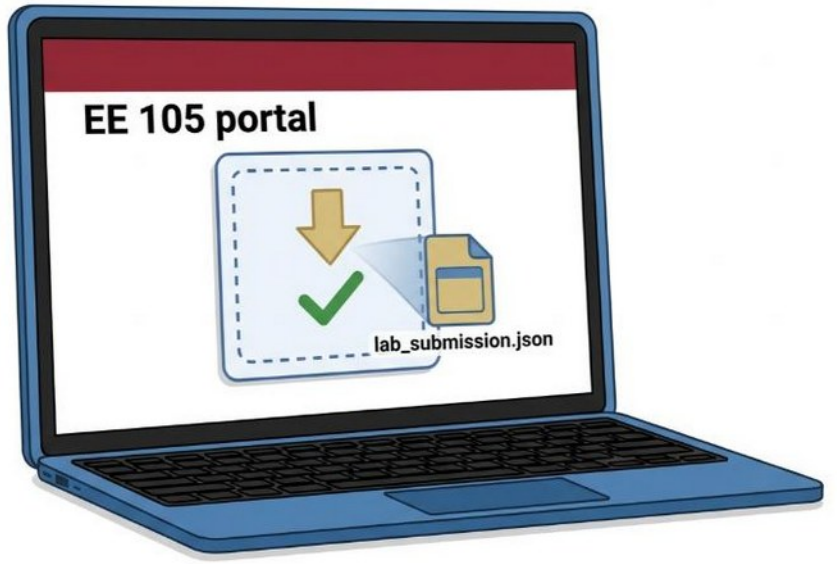
V_DS = V_DAC2 - I_D·R_path. Check r_path (C2) and id_vds (C3).

Submit your results

The last cell saves your results in one file. Upload it on the course portal.

`lab2.1_submission.json`

1. **Save · RUN** writes **lab2.1_submission.json** next to the notebook
2. It holds your fitted numbers and the raw sweeps behind them
3. Log in at **ee105.org/portal** with your student ID and portal PIN; open Lab 2.1
4. Upload: the portal recomputes the knee, R_path and the threshold from your sweeps



ee105.org/portal

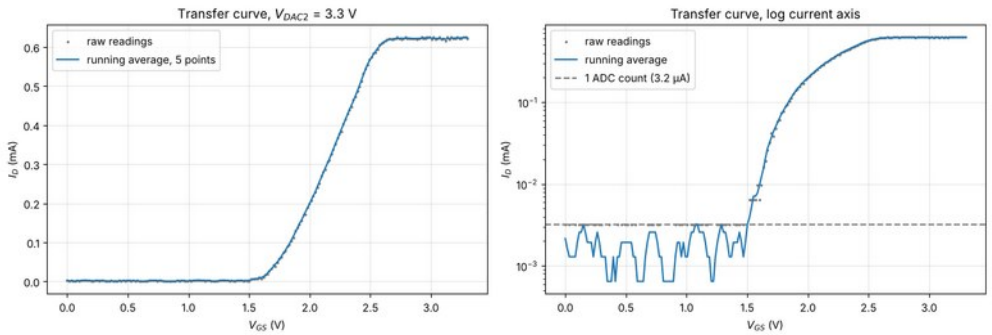
Check: the portal shows your grade. The three CSV files stay in the lab folder for your report. A simulated run earns no credit.

Lab complete

You measured the two devices every chip is built from.

You built:

- A 201-point diode I-V sweep and its knee voltage
- Two estimates of the ideality factor, and why they differ
- MOSFET transfer and output curves, and the drain path behind them
- V_th, K and V_DS,sat from your own smoothed data



Measure the circuit, not the schematic: this drain path stops the current at 0.62 mA.

Did you know?

The first transistor, built at Bell Labs on December 16, 1947, was a slab of germanium touched by two gold contacts (Chapter 2). A modern AI chip holds about 150 billion (Chapter 0).

Next

Lab 3.1, thermistor temperature sensor: turn a divider voltage into degrees. S10 back on Module 1.