USC University of Southern California

EE 105: Introduction to Electrical Engineering

Lecture 10

Device 2

Yasser Khan

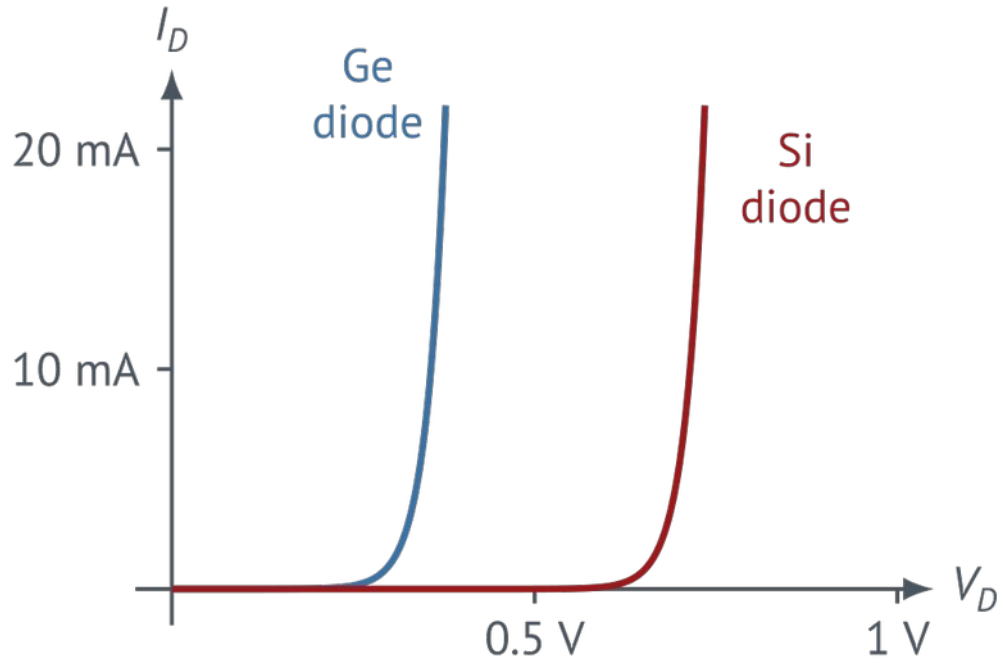
Rehan Kapadia

What is a diode

A diode passes current in one direction only: it rectifies.



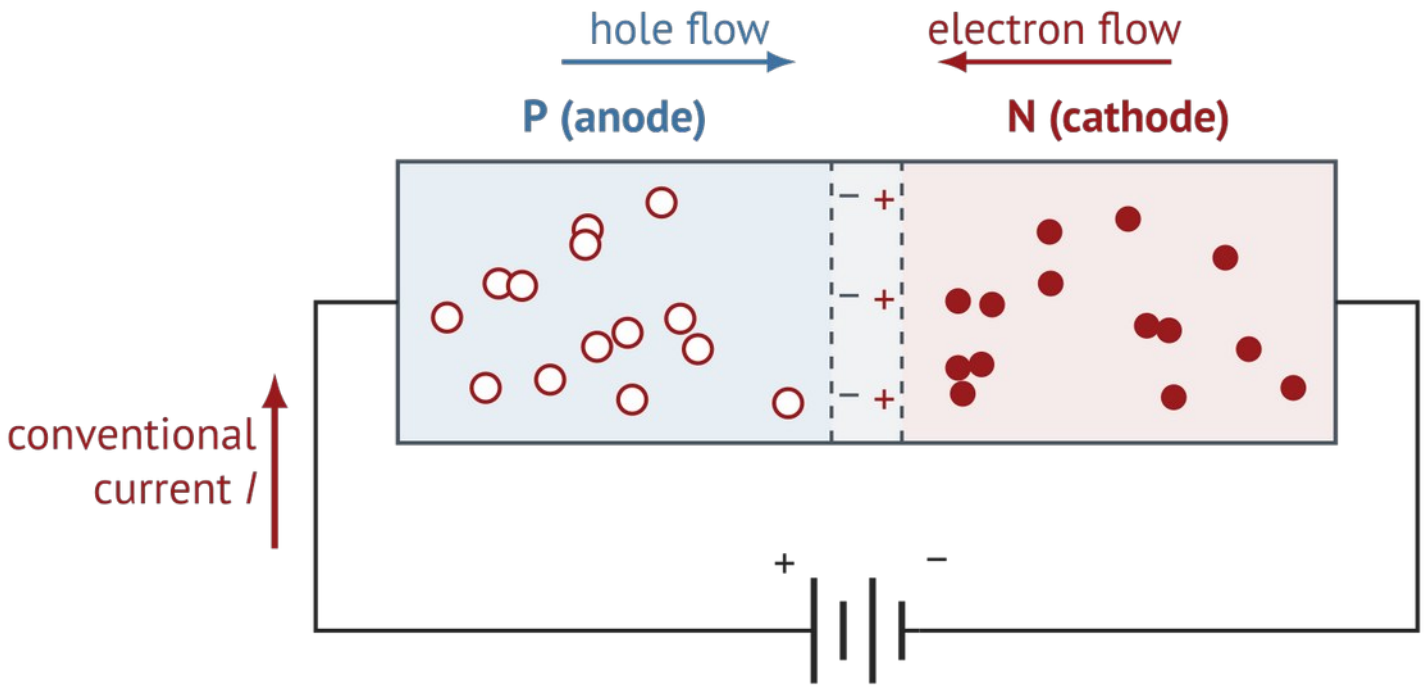


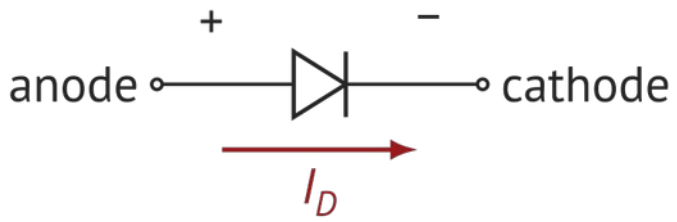


- A diode is a device that shows **rectifying** behavior: current flows easily one way only
- It can be made from a junction between an **n-type** and a **p-type** semiconductor (a pn junction)
- It can also be made from a metal-semiconductor junction (Schottky diode, not discussed here)

Forward biasing a diode

Anode positive: the barrier drops, carriers flood across the junction, and current flows ("open door").

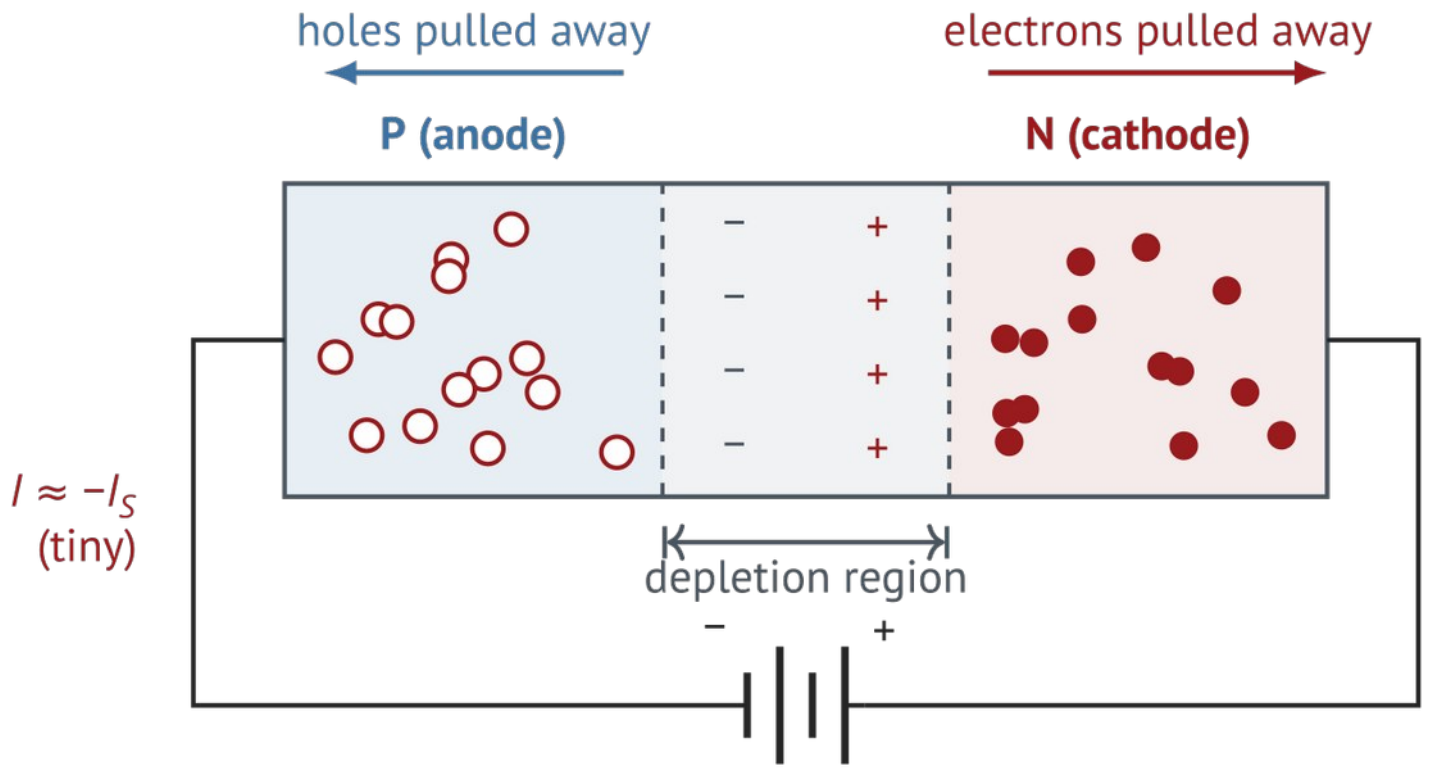




- Battery **+** on the p side (anode)
- Holes and electrons are pushed **toward** the junction; the depletion region **narrows**
- The barrier drops, so current rises **exponentially**: a large current flows

Reverse biasing a diode

Anode negative: carriers are pulled away, the depletion region widens, and the door closes.

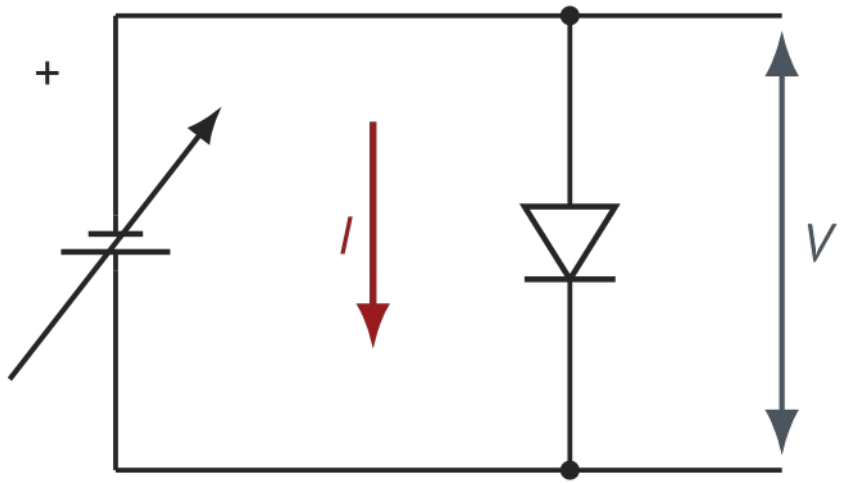


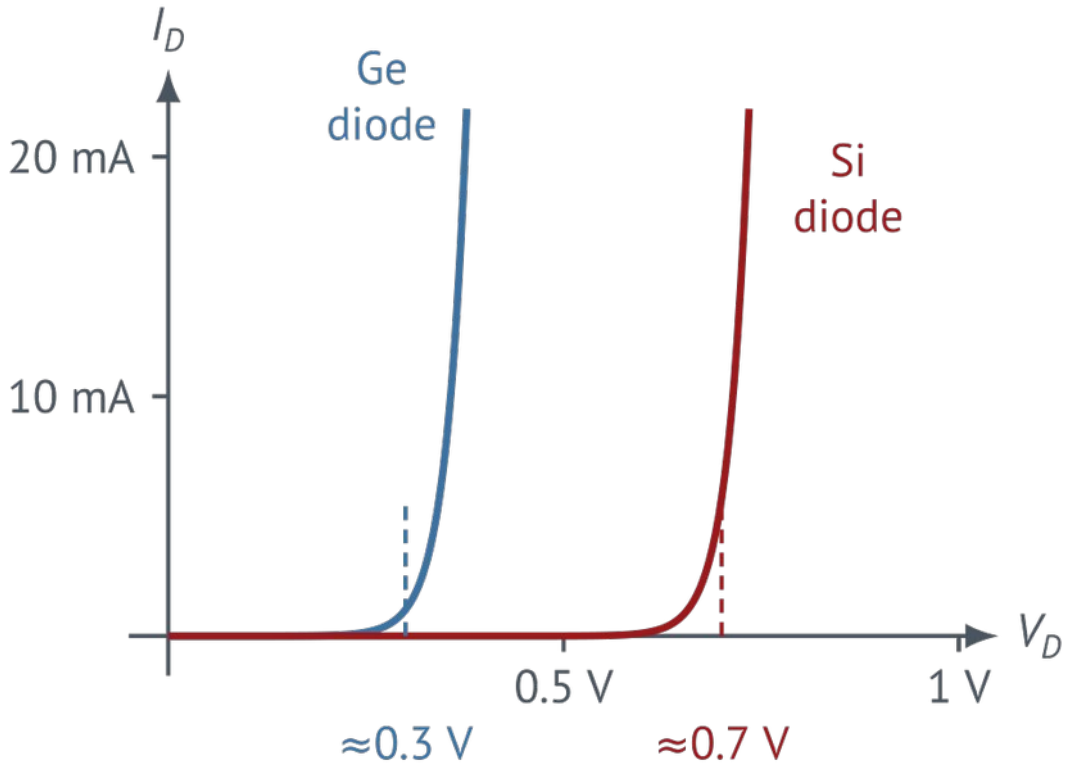


- Battery **–** on the p side (anode)
- Holes and electrons are pulled **away** from the junction; the depletion region **widens**
- Only a tiny leakage, $I \approx -I_S$, flows until breakdown

Diode characterization

Sweep the voltage across the diode and measure the current: nothing flows until the knee.

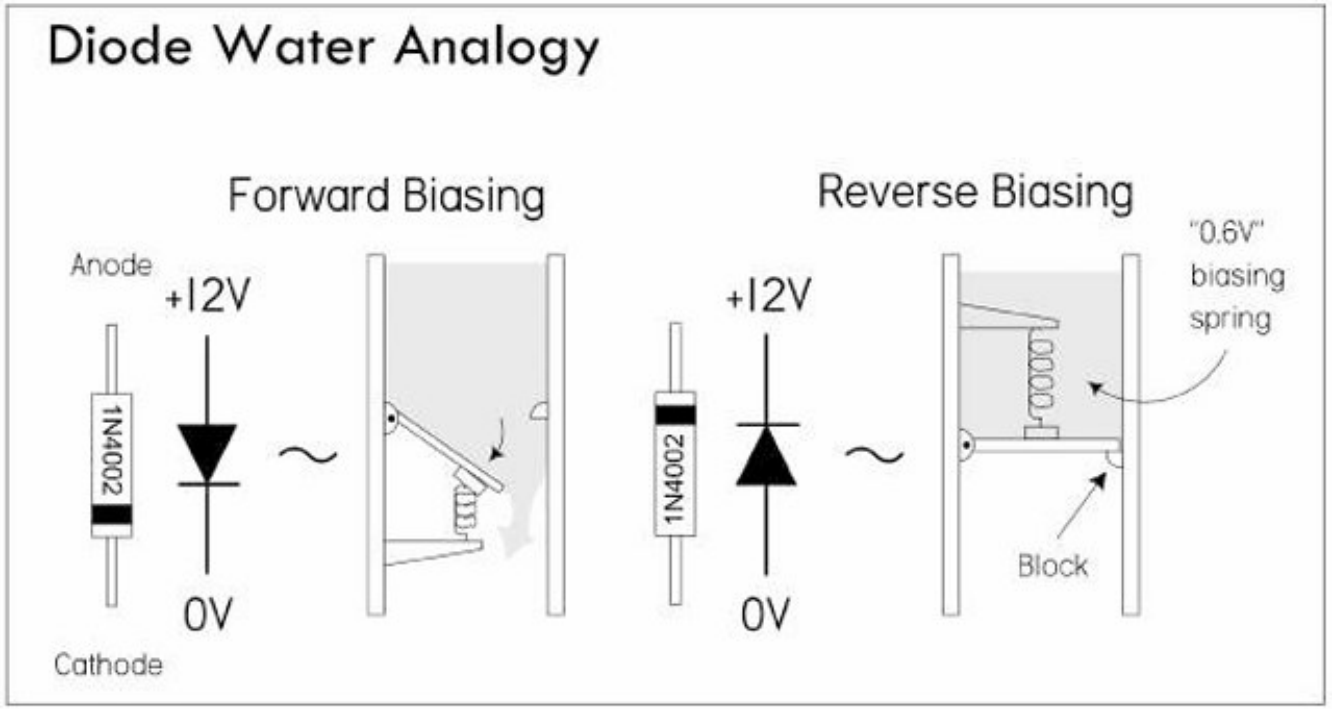


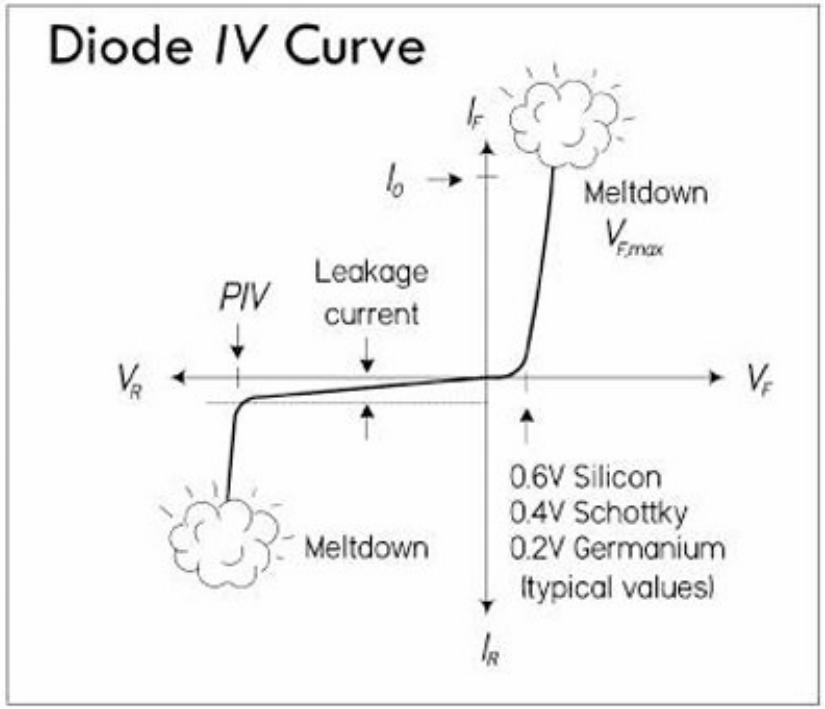


The knee (turn-on) voltage: about **0.3 V** for germanium, **0.6 to 0.7 V** for silicon, 1.6 to 3.5 V for visible LEDs.

Water analogy

A diode acts like a spring-loaded flap valve: it opens one way once the pressure beats the spring.





Forward bias

Pressure beats the "0.6 V" spring; the flap opens and current flows.

Reverse bias

The flap closes against its block; only a small leakage seeps through.

Breakdown

Too much reverse pressure (beyond the PIV) or forward current: meltdown.

Diode Current Equation

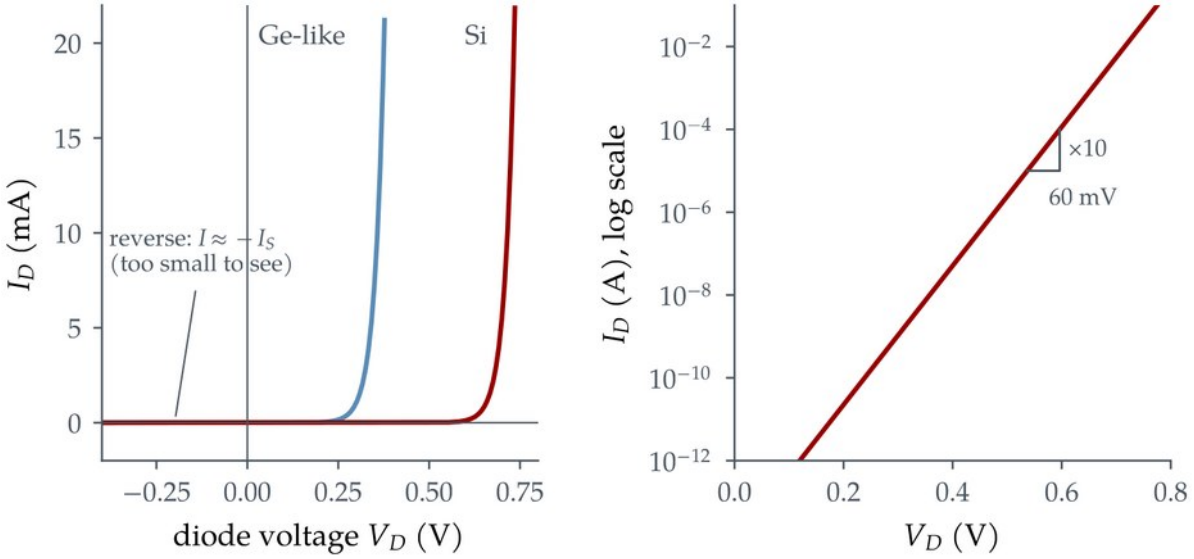
The diode equation: current grows exponentially with forward voltage, about 10× per 60 mV.

Diode (Shockley) equation

$$I_D = I_S\left(e^{V_D/nV_T} - 1\right)$$

same as $I = I_0\left(e^{qV/nkT} - 1\right), \quad V_T = \frac{kT}{q}$

- This equation **partially** describes a non-ideal diode
- It leaves out series resistance, extra reverse leakage, and breakdown



n = 1, V_T = 25.9 mV. Left: linear axes, Si ($I_S = 10^{-14}$ A) and a Ge-like diode (10^{-8} A). Right: log scale, one decade per 60 mV.

Diode Current Equation

Example 1: at 0.7 V the equation predicts half an ampere; a real circuit limits it far below that.

$$I_D = I_S\left(e^{V_D/nV_T} - 1\right)$$

where

- I_D: diode current, anode to cathode
- I_S: reverse saturation current (very small, e.g. 10^{-12} A)
- V_D: voltage across the diode, anode minus cathode
- n: ideality factor (≈ 1 for silicon)
- $V_T = kT/q \approx 25.9$ mV at 300 K (often rounded to 26 mV)

EXAMPLE

Example 1: forward bias at 0.7 V. Let $I_S = 10^{-12}$ A, n = 1, V_T = 0.026 V.

1. Exponent: 0.7/0.026 = 26.92
2. $e^{26.92} = 4.93 \times 10^{11}$
3. $I = 10^{-12} \times (4.93 \times 10^{11} - 1) \approx$ **0.49 A**

$$I = 10^{-12}\left(e^{0.7/0.026} - 1\right) \approx 0.49\ \text{A}$$

Too much for a small diode: in a circuit, a series resistor sets the current and V_D stays below 0.7 V.

Diode Current Equation

Examples 2 to 4: a 0.1 V change multiplies the forward current by 47; reverse current is just $-I_S$.

EXAMPLE

Example 2: forward bias, 0.6 V

1. 0.6/0.026 = 23.08
2. $e^{23.08} = 1.05 \times 10^{10}$
3. $I \approx 10^{-12} \times 1.05 \times 10^{10} =$ **10.5 mA**

EXAMPLE

Example 3: reverse bias, −5 V

1. −5/0.026 = −192
2. $e^{-192} \approx 0$
3. $I \approx 10^{-12} \times (0 - 1) =$ **-10^{-12} A** $= -I_S$

EXAMPLE

Example 4: small voltage, 0.1 V

1. 0.1/0.026 = 3.85
2. $e^{3.85} = 46.8$
3. $I \approx 10^{-12} \times (46.8 - 1) =$ **4.58×10^{-11} A**

Same $I_S = 10^{-12}$ A, n = 1, $V_T = 0.026$ V in all three

$$I = 10^{-12}\,(e^{V/0.026} - 1)$$

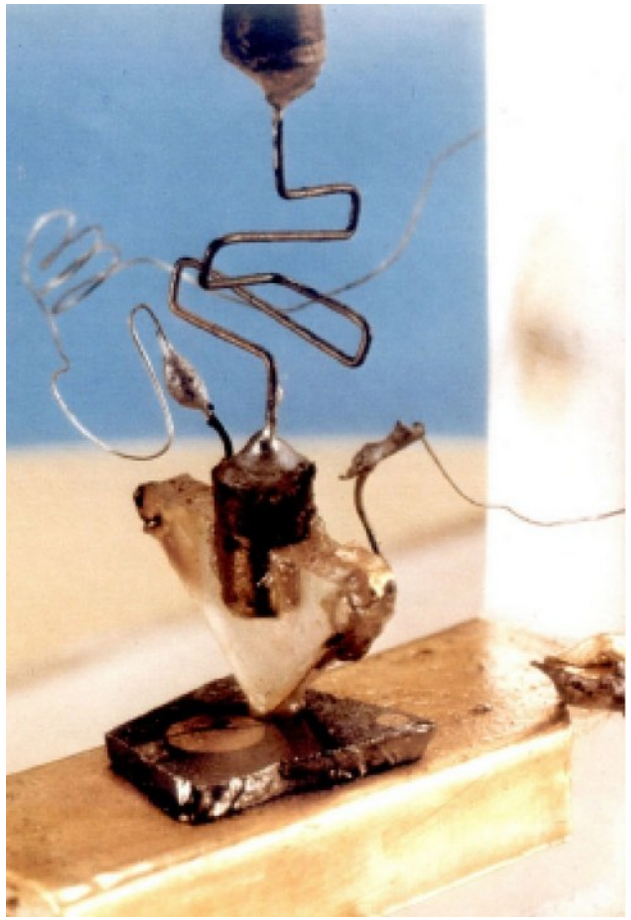
0.6 V → 0.7 V multiplies I by $e^{0.1/0.026} =$ **47**: a conducting diode stays near 0.6 to 0.7 V.

The First Transistor

December 16, 1947: a slab of germanium with two gold contacts amplified a signal at Bell Labs.

Bell Telephone Laboratories

- Goal: a **solid-state amplifier** for telephone signals
- **John Bardeen** (theorist)
- **Walter Brattain** (experimentalist)
- **William Shockley** (team leader, physicist)



The first point-contact transistor, Bell Labs, 1947

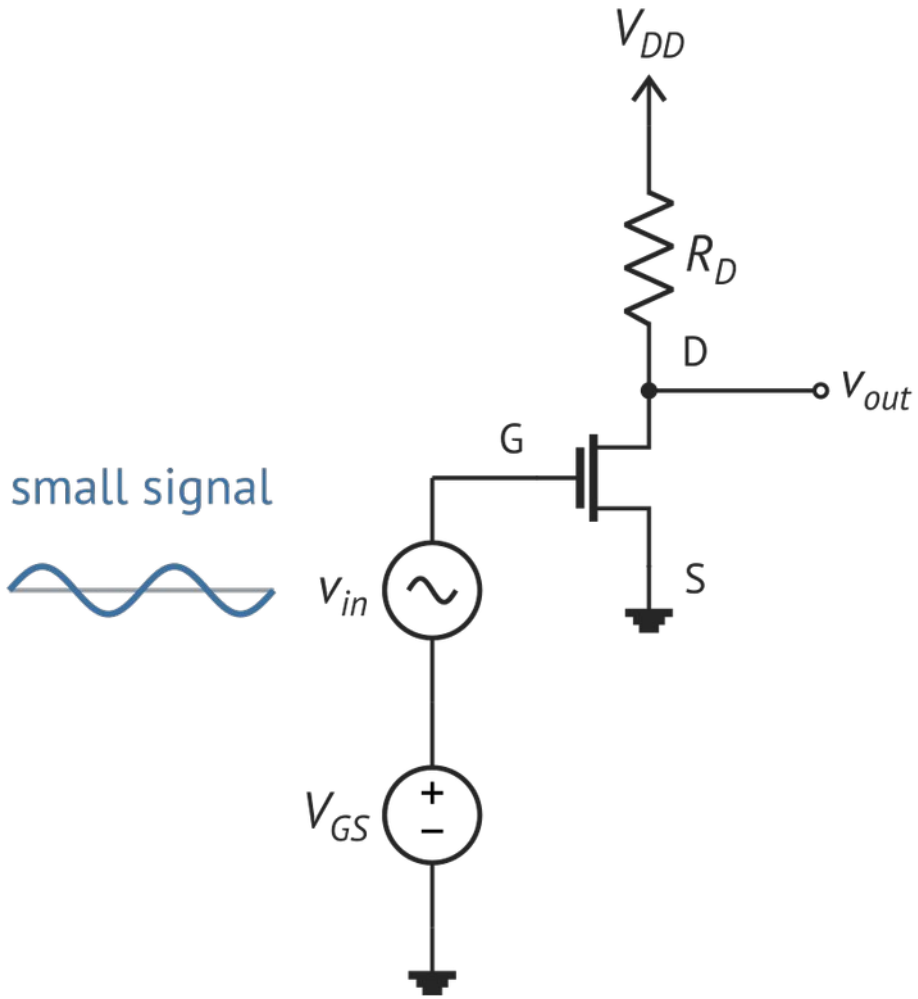
Point-contact transistor

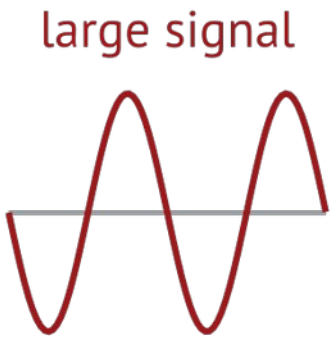
- A small slab of **germanium** with two closely spaced **gold contacts**
- Current into one contact changes the germanium's conductivity, **amplifying** the signal at the other

Key outcome: it amplified like a vacuum tube, in a device a few millimeters wide.

Transistor amplification

A small signal on the gate steers a large drain current, and R_D turns it into a large output swing.





Voltage gain

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D$$

- The gate voltage sets the drain current
- R_D converts the current change into a voltage change
- Inverted, and larger: **amplified**

1956 Physics Nobel Prize

Shockley, Bardeen, and Brattain shared the prize "for their researches on semiconductors".

"for their researches on semiconductors and their discovery of the transistor effect"



William Bradford Shockley

1/3 of the prize

USA

Semiconductor Laboratory of Beckman Instruments, Inc.
Mountain View, CA, USA



John Bardeen

1/3 of the prize

USA

University of Illinois
Urbana, IL, USA



Walter Houser Brattain

1/3 of the prize

USA

Bell Telephone Laboratories
Murray Hill, NJ, USA

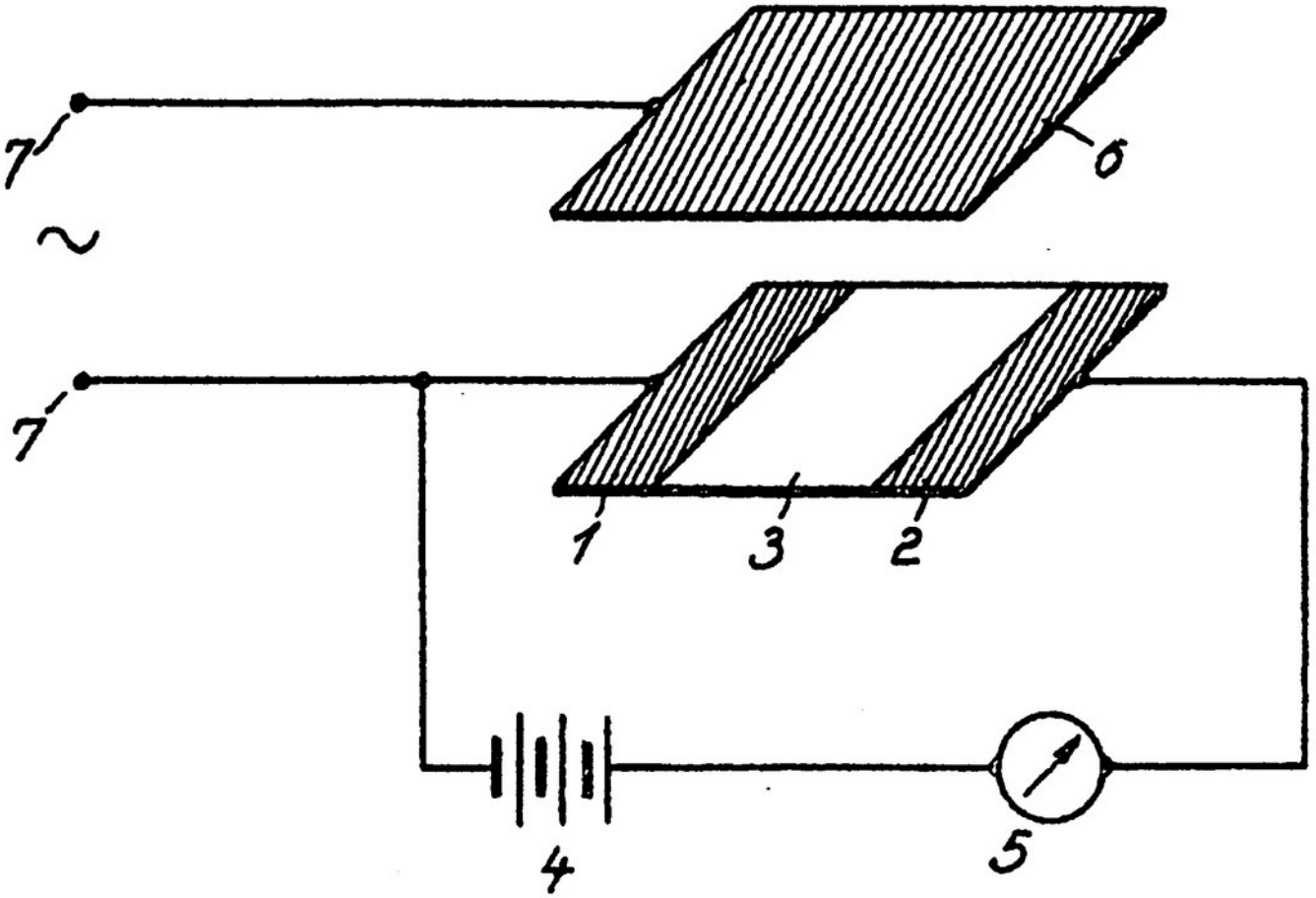
"for their researches on semiconductors and their discovery of the transistor effect"

- **William Shockley**: Beckman Instruments, Mountain View, CA
- **John Bardeen**: University of Illinois, Urbana, IL
- **Walter Brattain**: Bell Telephone Laboratories, Murray Hill, NJ

1/3 of the prize each

Invention of the Field-Effect Transistor

The field-effect idea is older than the transistor: Oskar Heil patented it in 1935.



Drawing from Oskar Heil's 1935 British patent

- **1935**: a British patent is issued to **Oskar Heil**
- Idea: a voltage on a plate controls the conductance of a semiconductor layer beneath it
- A working MOSFET came only after clean SiO_2 could be grown on silicon (**1955 to 1960**)

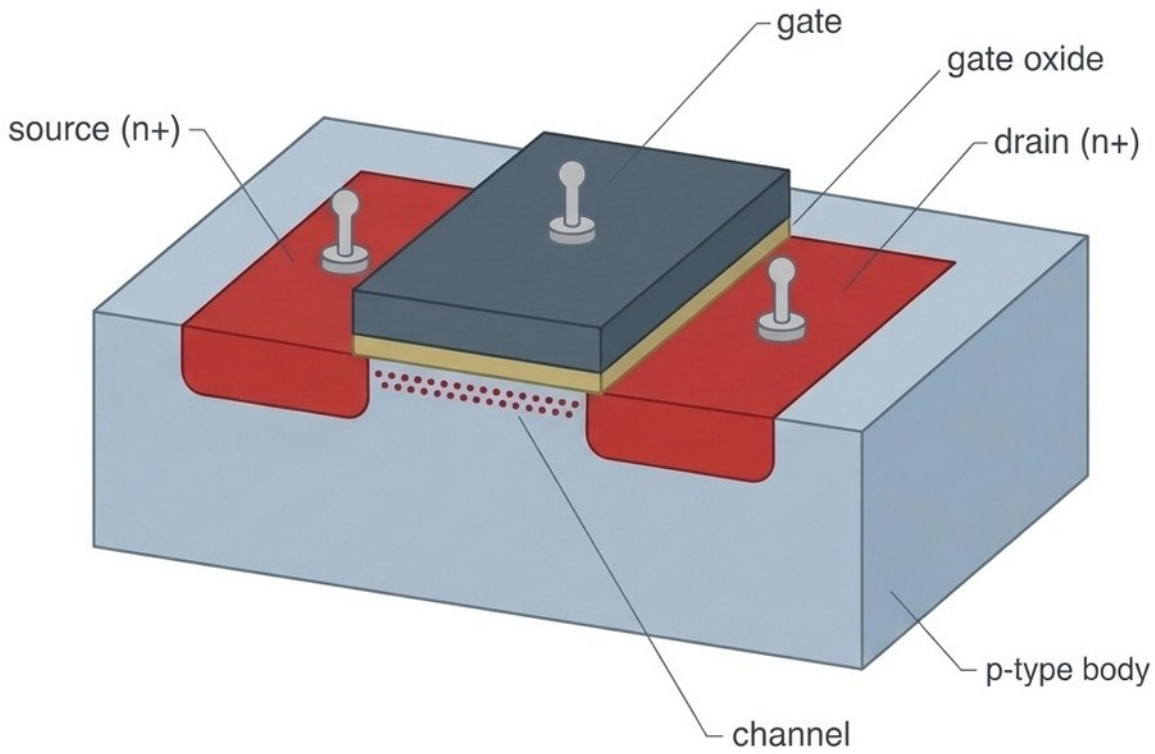
Modern Field Effect Transistor (FET)

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A voltage on the gate sets the conductance of the silicon beneath it, and so the source-drain current.

- An **electric field** is applied normal to the semiconductor surface, by a voltage on an overlying electrode, to modulate the **conductance** of the semiconductor
- → This modulates the **drift current** between two contacts, the **source** and the **drain**, as the voltage on the **gate** changes

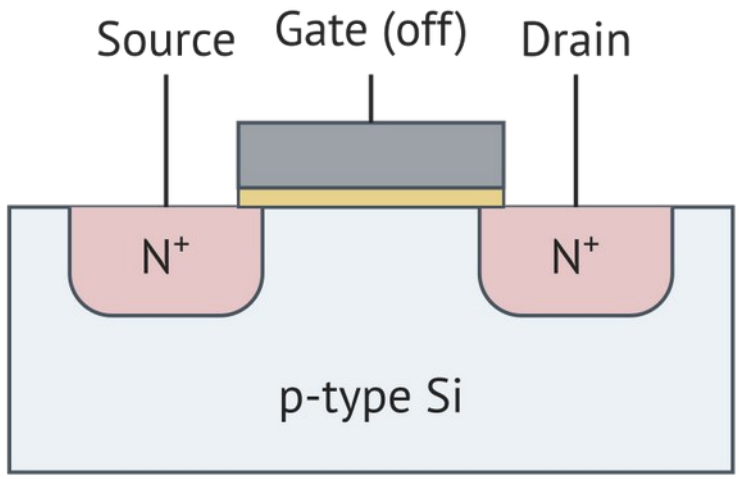
Gate, oxide, silicon: the layers give the MOSFET its name (metal-oxide-semiconductor).



N-channel MOSFET: n+ source and drain in a p-type body, gate on a thin oxide

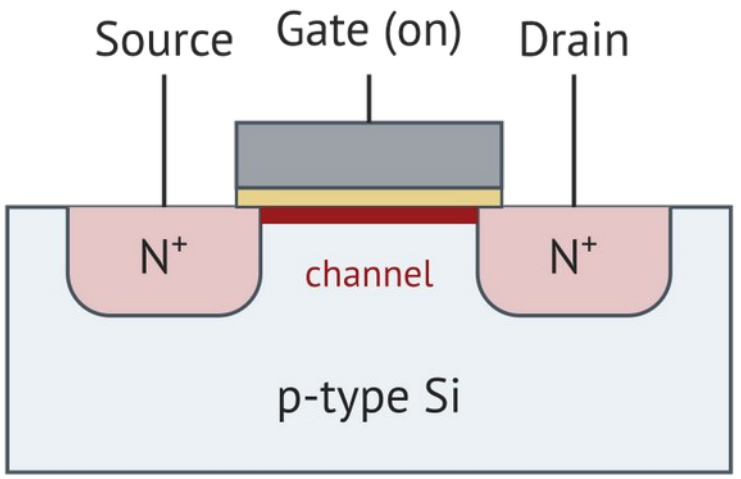
MOSFET: metal-oxide-semiconductor field-effect transistor

The gate changes the resistance of the channel: no channel blocks current, a channel lets it flow.





high resistance
no flow



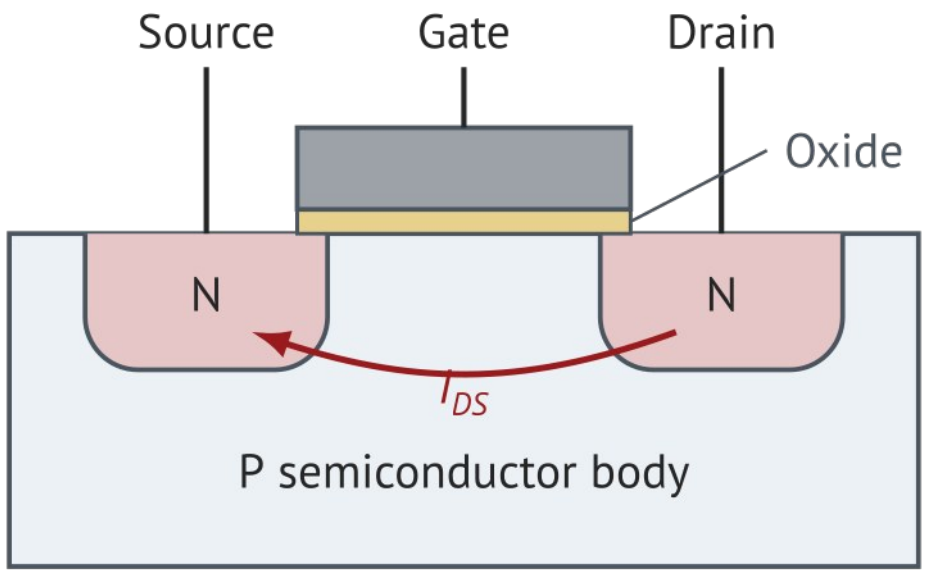


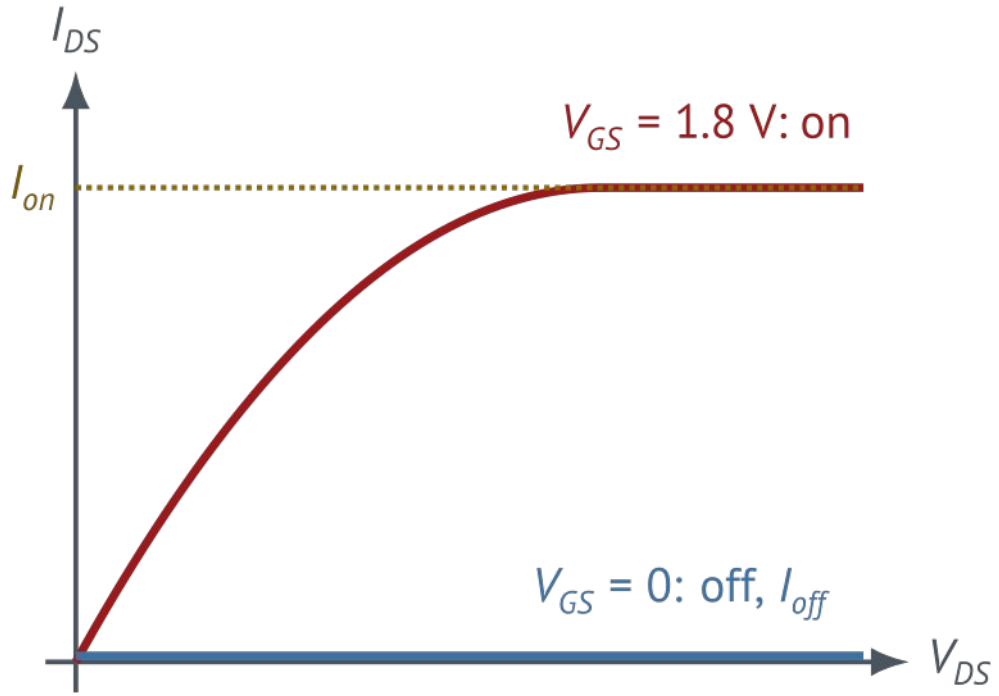
low resistance
high flow

Metal (gate) · **O**xide (insulator) · **S**emiconductor (silicon) · **F**ield-**E**ffect **T**ransistor: the gate's field changes the channel resistance

Introduction to the MOSFET

Basic structure and I-V: the gate voltage switches the drain current between I_{on} and I_{off}.





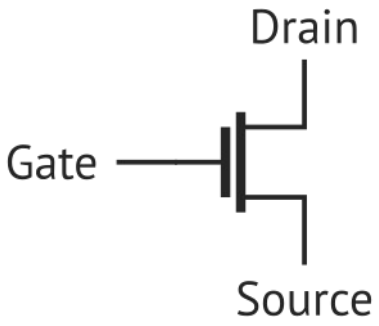
- I_{DS}: current from drain to source
- V_{DS}: voltage between drain and source

What is desirable: **large I_{on}, small I_{off}**

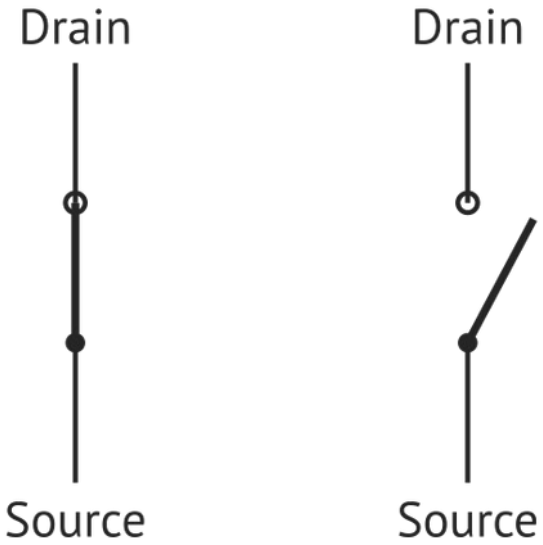
Introduction to the MOSFET

Two ways of representing a MOSFET: its circuit symbol, and a switch that the gate opens and closes.

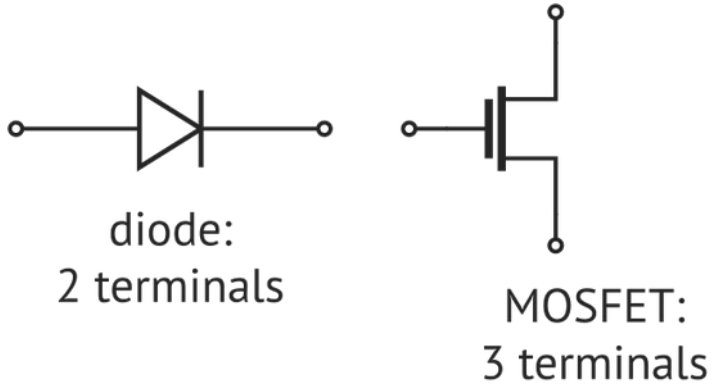
Circuit symbol (NMOS)



Simple switch



Two terminals vs three



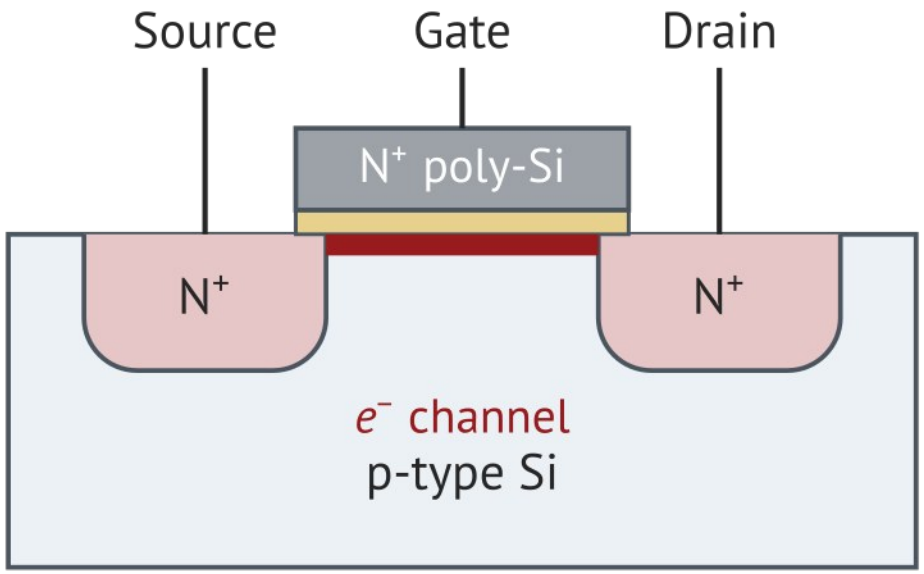
n-channel (NMOS): on when $V_{GS} > V_{th}$. **p-channel (PMOS):** on when $V_{GS} < V_{th}$ ($V_{th} < 0$).

The gate is a third terminal: it controls the current between drain and source.

N-channel vs. P-channel

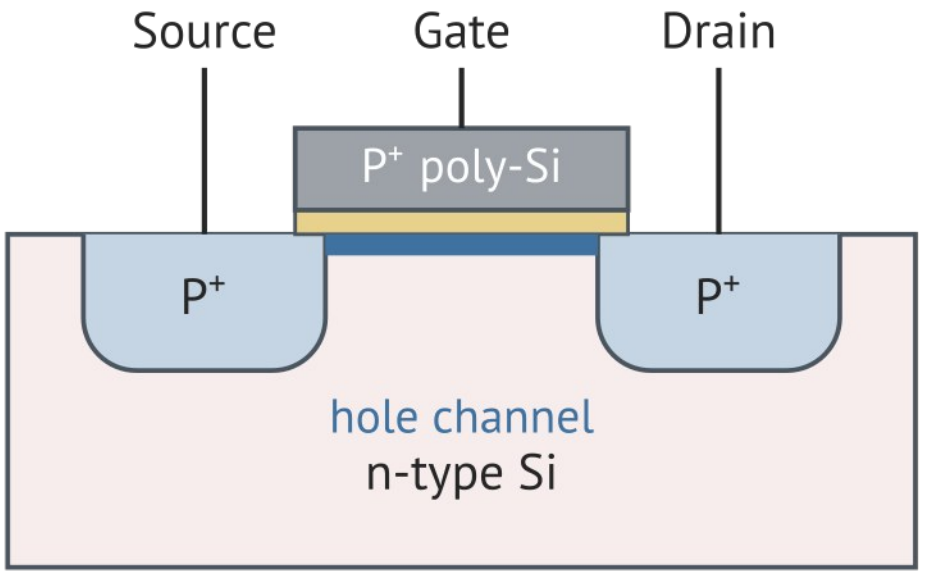
Swap every doping type to get the PMOS: n-type body, p+ source and drain, and a channel of holes.

NMOS (n-channel)



- For current to flow: $\mathbf{V_{GS} > V_{th}}$ (positive gate)
- Enhancement mode: $V_{th} > 0$

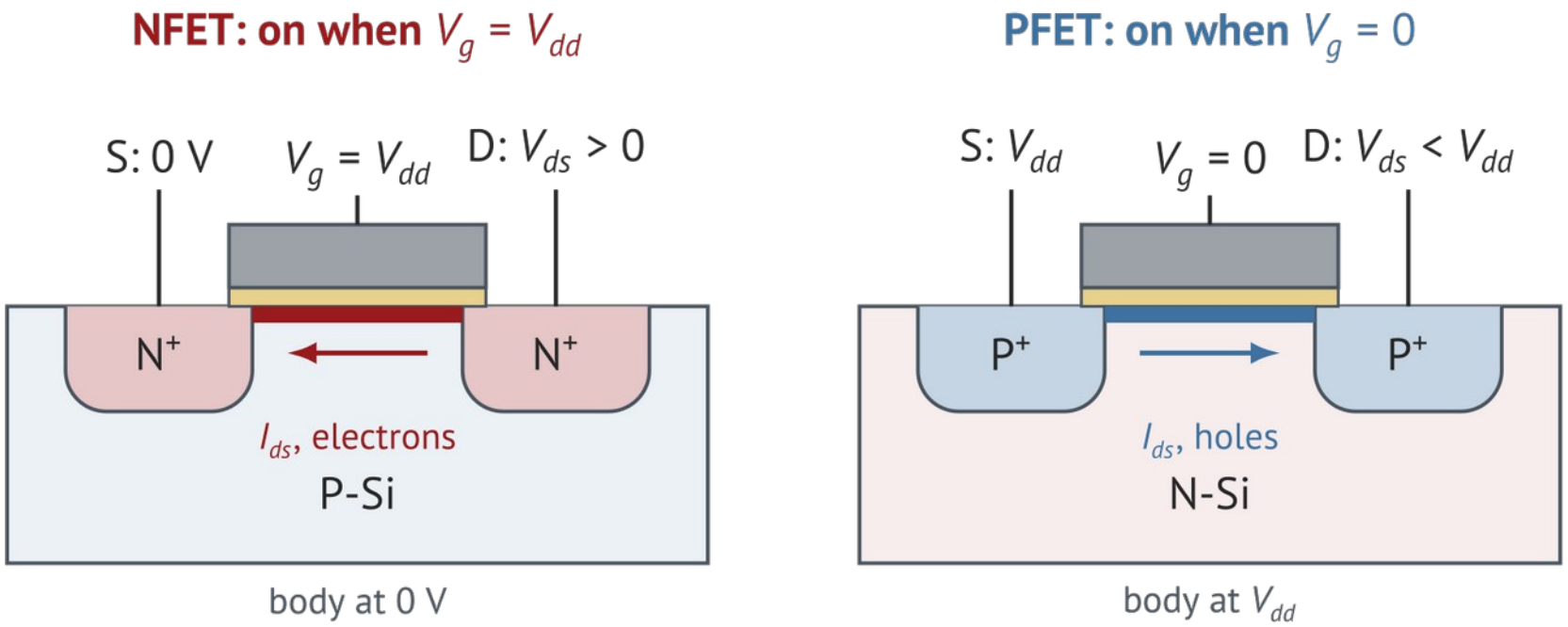
PMOS (p-channel)



- For current to flow: $\mathbf{V_{GS} < V_{th}}$ (negative gate)
- Enhancement mode: $V_{th} < 0$

Complementary MOSFETs (CMOS)

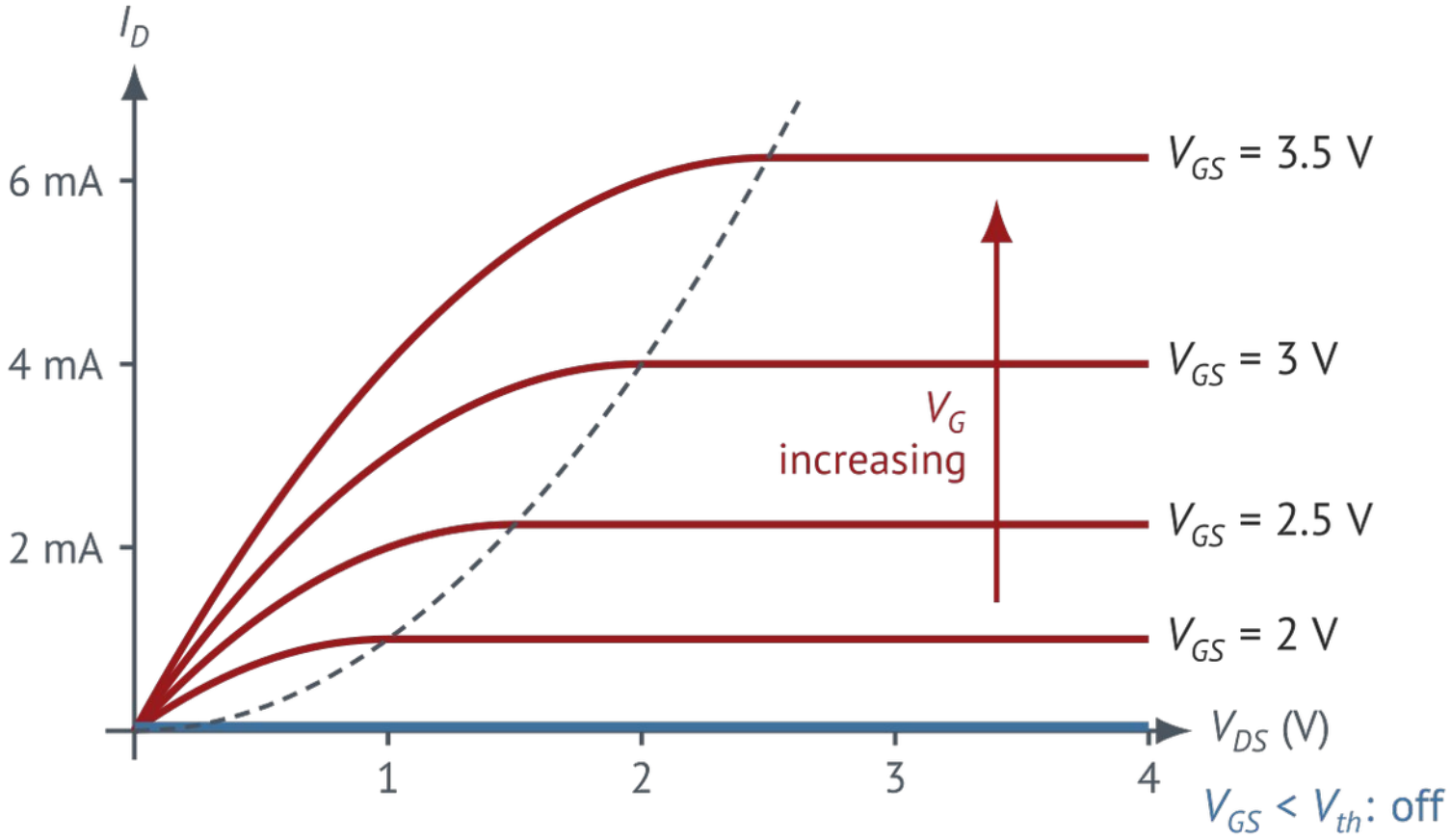
One gate voltage turns one device on and the other off: that complementary pair is CMOS.



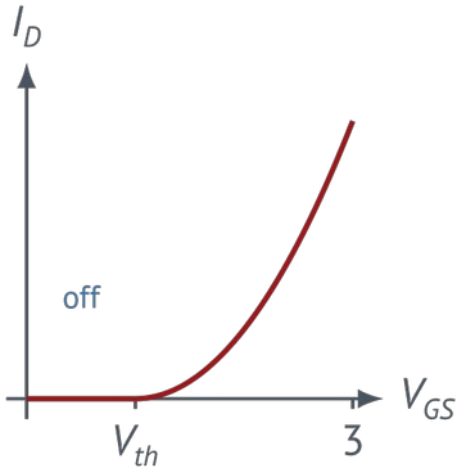
Gate voltage	NFET (source at 0)	PFET (source at V_{dd})
$V_g = V_{dd}$	**on** (electron channel)	off
$V_g = 0$	off	**on** (hole channel)

I_D-V_{DS} characteristics of a long-channel n-MOSFET

Expected for a long channel ($\Delta L \ll L$), for several gate voltages: each V_G gives one curve.



Transfer curve (saturation)



- $V_G > V_T$: I_D rises, then saturates
- $V_G < V_T$: no channel, $I_D \approx 0$ (**off**)

Dashed: $V_{DS} = V_{GS} - V_{th}$, where saturation begins

MOSFET current equations

Two equations, one for each region; one device constant k' = $\mu_n C_{ox} W/L$ sets the scale.

Linear (triode) region: $V_{DS} < V_{GS} - V_{th}$

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{th}) V_{DS} - \tfrac{1}{2} V_{DS}^2]$$

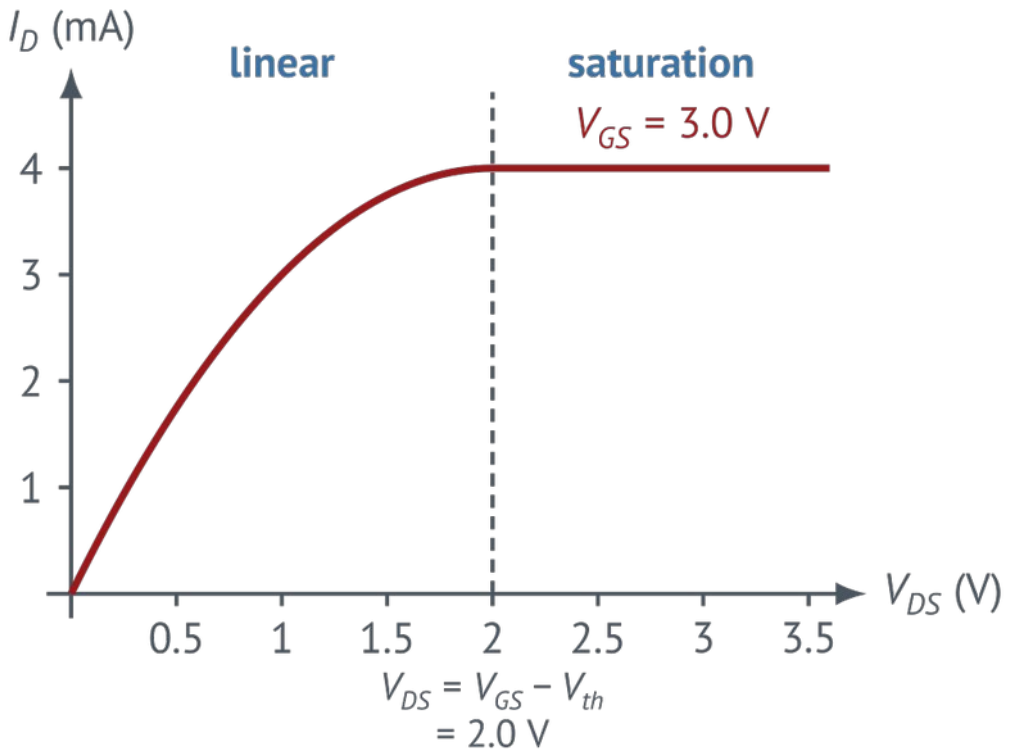
Saturation region: $V_{DS} \geq V_{GS} - V_{th}$

$$I_D = \tfrac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

Assume device parameters

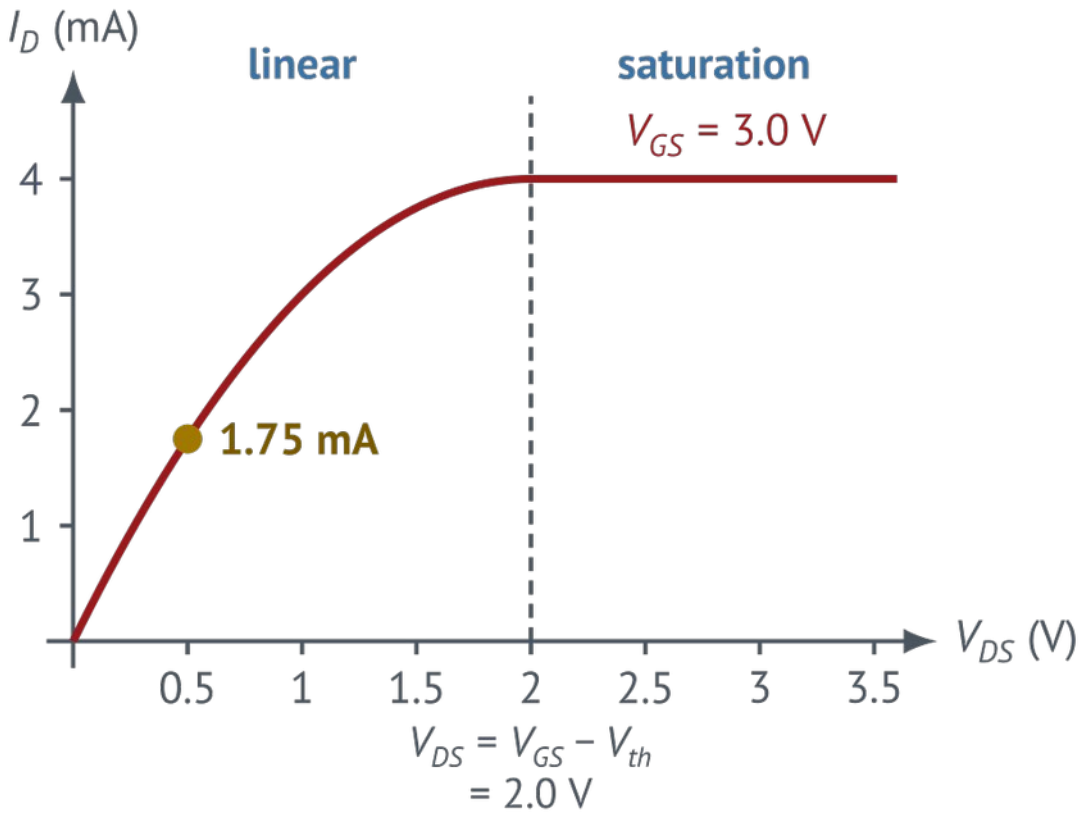
- $\mu_n C_{ox} = 200\ \mu A/V^2$
- $W/L = 10$
- $V_{th} = 1.0\ V$

$$k' = \mu_n C_{ox} \frac{W}{L} = 200 \times 10 = 2\ mA/V^2$$



MOSFET current equations

Example 1: V_{DS} = 0.5 V is below the overdrive, so use the linear-region equation: 1.75 mA.



EXAMPLE

Example 1: linear region. V_{GS} = 3.0 V, V_{DS} = 0.5 V; k' = 2 mA/V², V_{th} = 1.0 V

1. Overdrive: $V_{GS} - V_{th} = 2.0$ V
2. Region: $V_{DS} = 0.5 < 2.0$, so the device is **linear**
3. $I_D = 2[(2.0)(0.5) - ½(0.5)^2] = 2[1.0 - 0.125] = 2 \times 0.875$

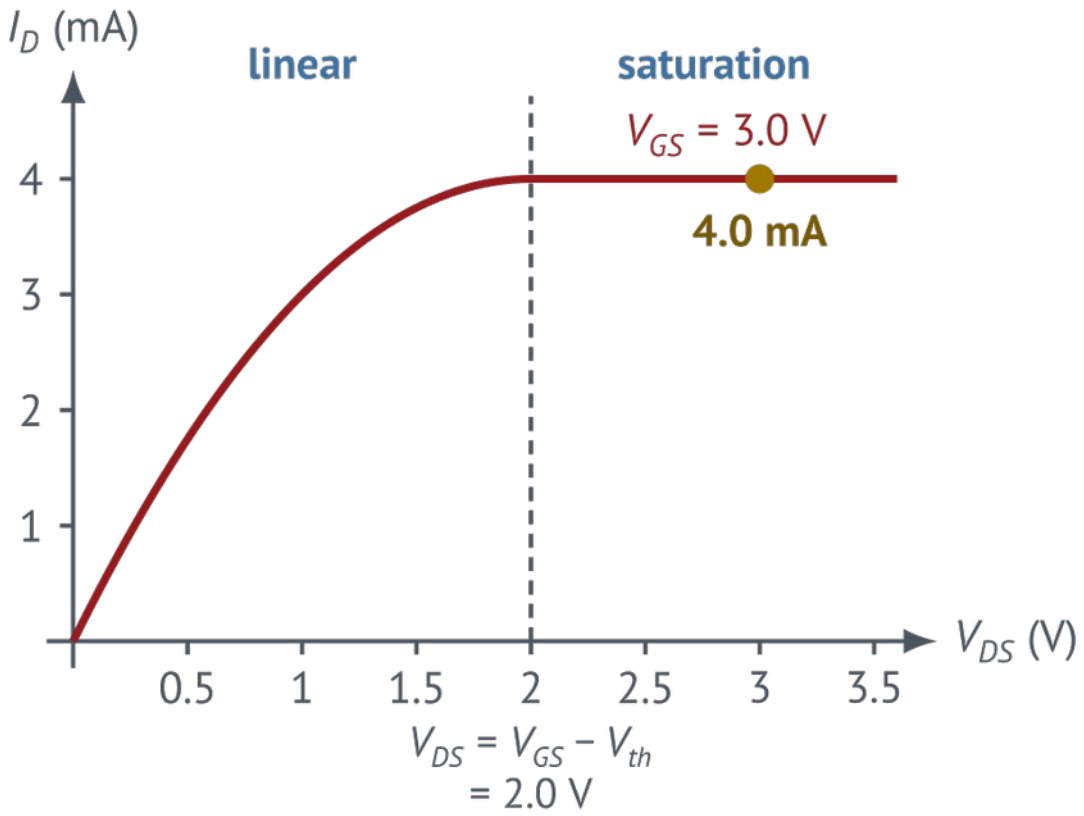
Linear region

$$I_D = 1.75 \text{ mA}$$

Device: $\mu_n C_{ox}$ = 200 µA/V², W/L = 10, so k' = 2 mA/V²

MOSFET current equations

Example 2: V_{DS} = 3.0 V is past the overdrive, so the device is saturated: 4.0 mA.



EXAMPLE

Example 2: saturation region. V_{GS} = 3.0 V, V_{DS} = 3.0 V; k' = 2 mA/V², V_{th} = 1.0 V

1. Overdrive: $V_{GS} - V_{th}$ = 2.0 V
2. Region: V_{DS} = 3.0 ≥ 2.0, so the device is **saturated**
3. $I_D = ½ \times 2 \times (2.0)^2 = 1 \times 4.0$

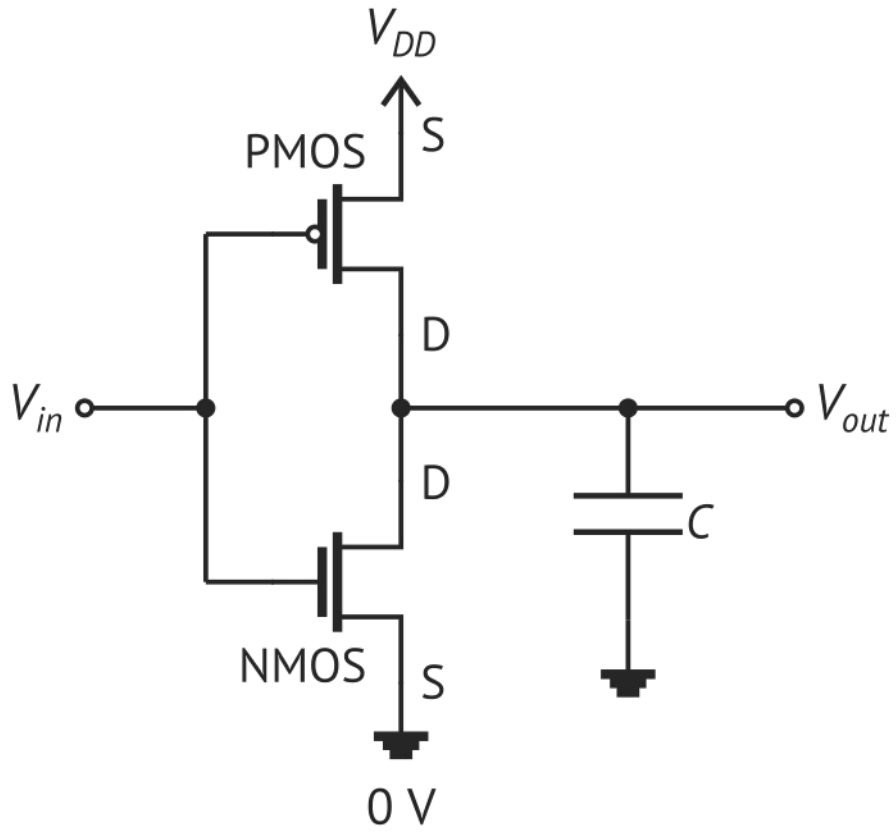
Saturation current

$$I_{D,sat} = 4.0 \text{ mA}$$

Device: $\mu_n C_{ox}$ = 200 µA/V², W/L = 10, so k' = 2 mA/V²

CMOS (Complementary MOS) Inverter

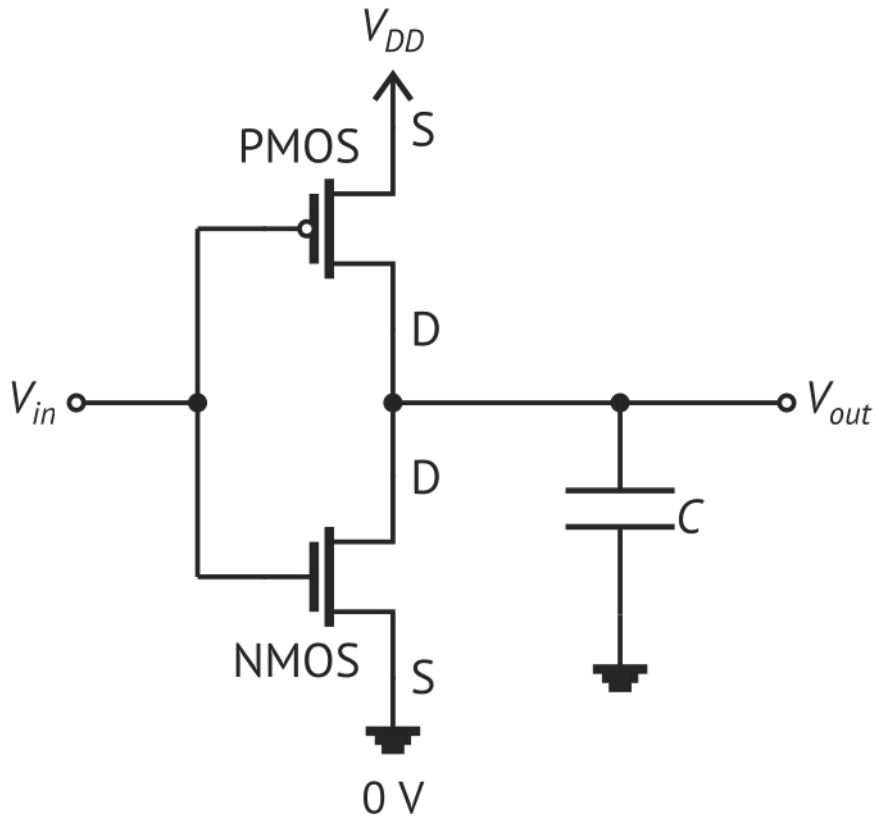
A PMOS pull-up and an NMOS pull-down share one input; their joined drains are the output.

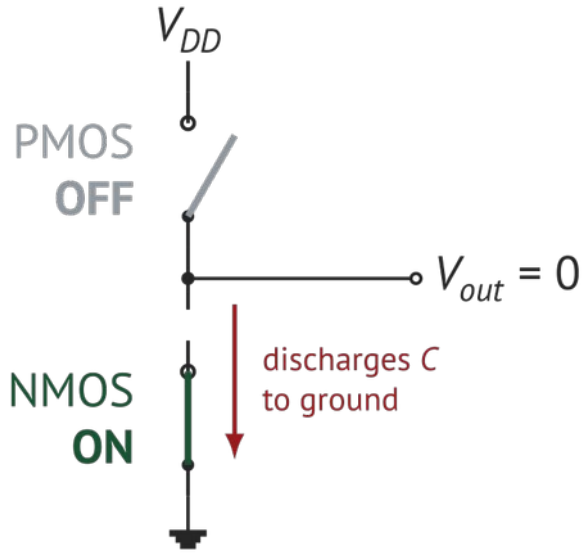


- **PMOS** on top: source at V_{DD}
- **NMOS** below: source at 0 V
- Gates joined: the input $\mathbf{V}_{in}$
- Drains joined: the output $\mathbf{V}_{out}$
- **C**: capacitance of the interconnect and of the next gates

CMOS (Complementary MOS) Inverter

Input high ($V_{in} = V_{DD}$): the NMOS is on, the PMOS is off, and the output falls to 0 V.





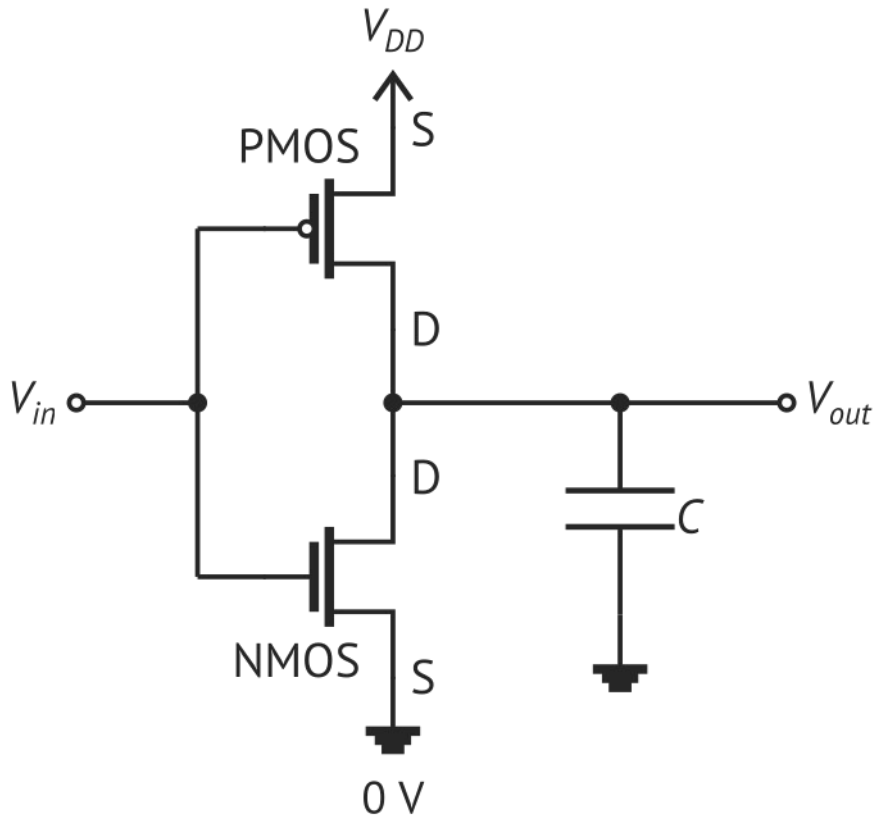
Truth table

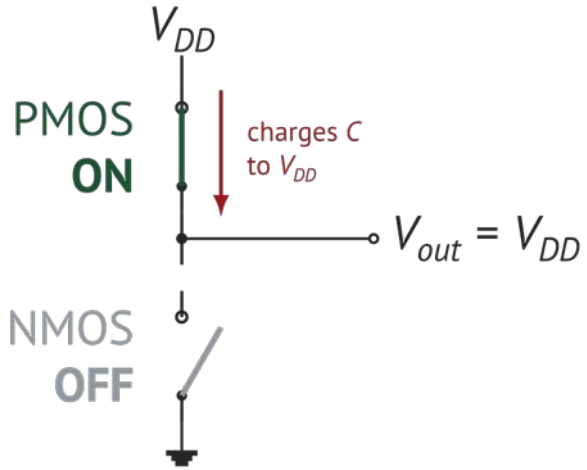
V_{in}	PMOS	NMOS	V_{out}
V_{DD}	off	on	**0 V**
0			?

NMOS: $V_{GS} = V_{DD} > V_{th}$, **on**. PMOS: $V_{GS} = 0$, **off**. Output pulled to ground.

CMOS (Complementary MOS) Inverter

Input low (V_{in} = 0): the PMOS is on, the NMOS is off, and the output rises to V_{DD}.





Truth table

V_{in}	PMOS	NMOS	V_{out}
V_{DD}	off	on	0 V
0	on	off	V_{DD}

PMOS: $V_{GS} = -V_{DD}$, **on**. NMOS: $V_{GS} = 0 < V_{th}$, **off**. Output pulled up to V_{DD}.

CMOS (Complementary MOS) Inverter

The output is the logical NOT of the input, and in either state no current flows from V_{DD} to ground.

Truth table (NOT gate)

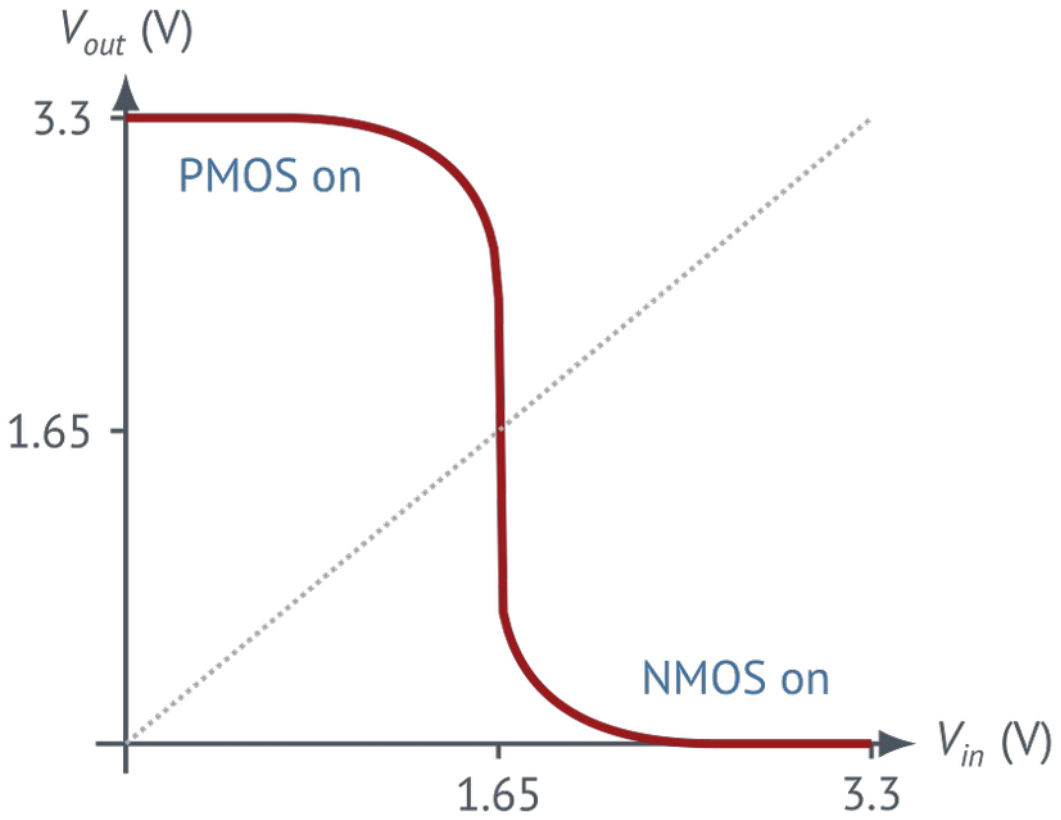
V_{in}	PMOS	NMOS	V_{out}
V_{DD}	off	on	0 V
0	on	off	V_{DD}

- One transistor is always **off**: no static current from V_{DD} to ground
- Power is used only when switching, to charge C

Dynamic power

$$P_{dyn} = C V_{DD}^2 f$$

Voltage transfer curve (V_{DD} = 3.3 V)



Qualitative discussion: n-MOSFET

As V_{DS} grows, the channel thins at the drain end until it pinches off and the current saturates.

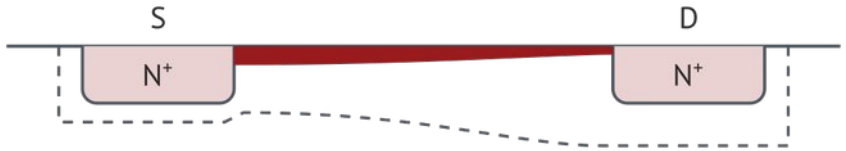
(a)



$V_{GS} > V_{th}$; $V_{DS} \approx 0$

I_D increases with V_{DS}

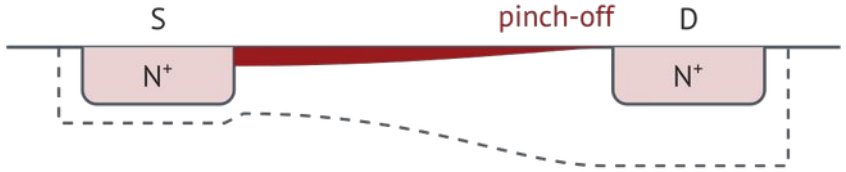
(b)



$V_{GS} > V_{th}$; V_{DS} small, > 0

I_D increases with V_{DS}, but the rate of increase decreases

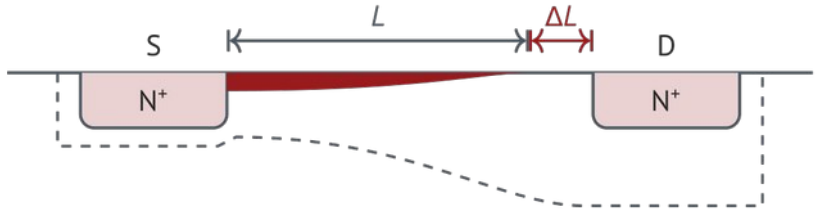
(c)



$V_{GS} > V_{th}$; V_{DS} at pinch-off

I_D reaches its saturation value $I_{D,sat}$; this V_{DS} is $V_{DS,sat}$

(d)



$V_{GS} > V_{th}$; $V_{DS} > V_{DS,sat}$

I_D does not increase further: the saturation region

Quantitative I_D-V_{DS} Relationships: "Square Law"

First attempt: the current rises with V_{DS} until pinch-off at $V_{DS,sat} = V_{GS} - V_{th}$, then stays flat.

$0 < V_{DS} < V_{DS,sat}$; $V_{GS} > V_{th}$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

- I_D increases with V_{DS} until $\mathbf{V_{GS} - V_{DS} = V_{th}}$: the channel **pinches off** at the drain

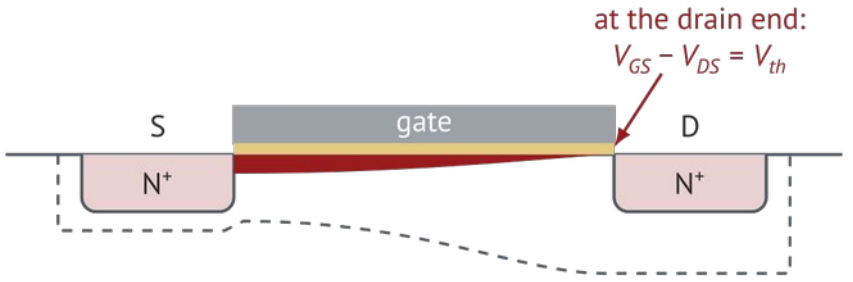
$V_{DS} \geq V_{DS,sat}$; $V_{GS} > V_{th}$

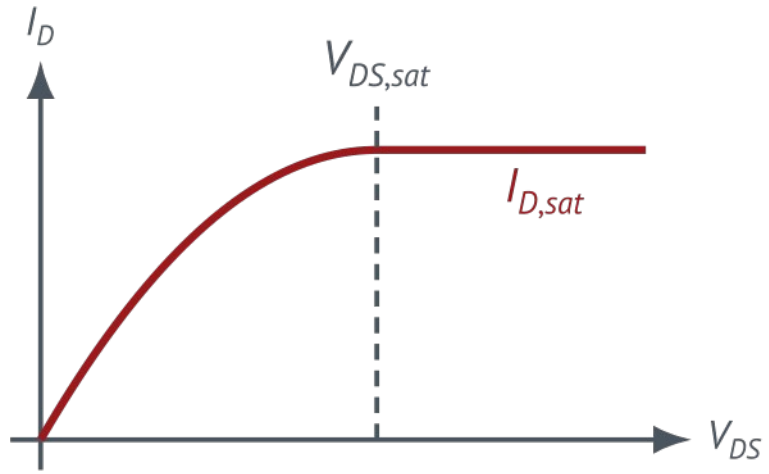
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

Oxide capacitance per unit area

$$C_{ox} = \varepsilon_{ox} / x_{ox}$$

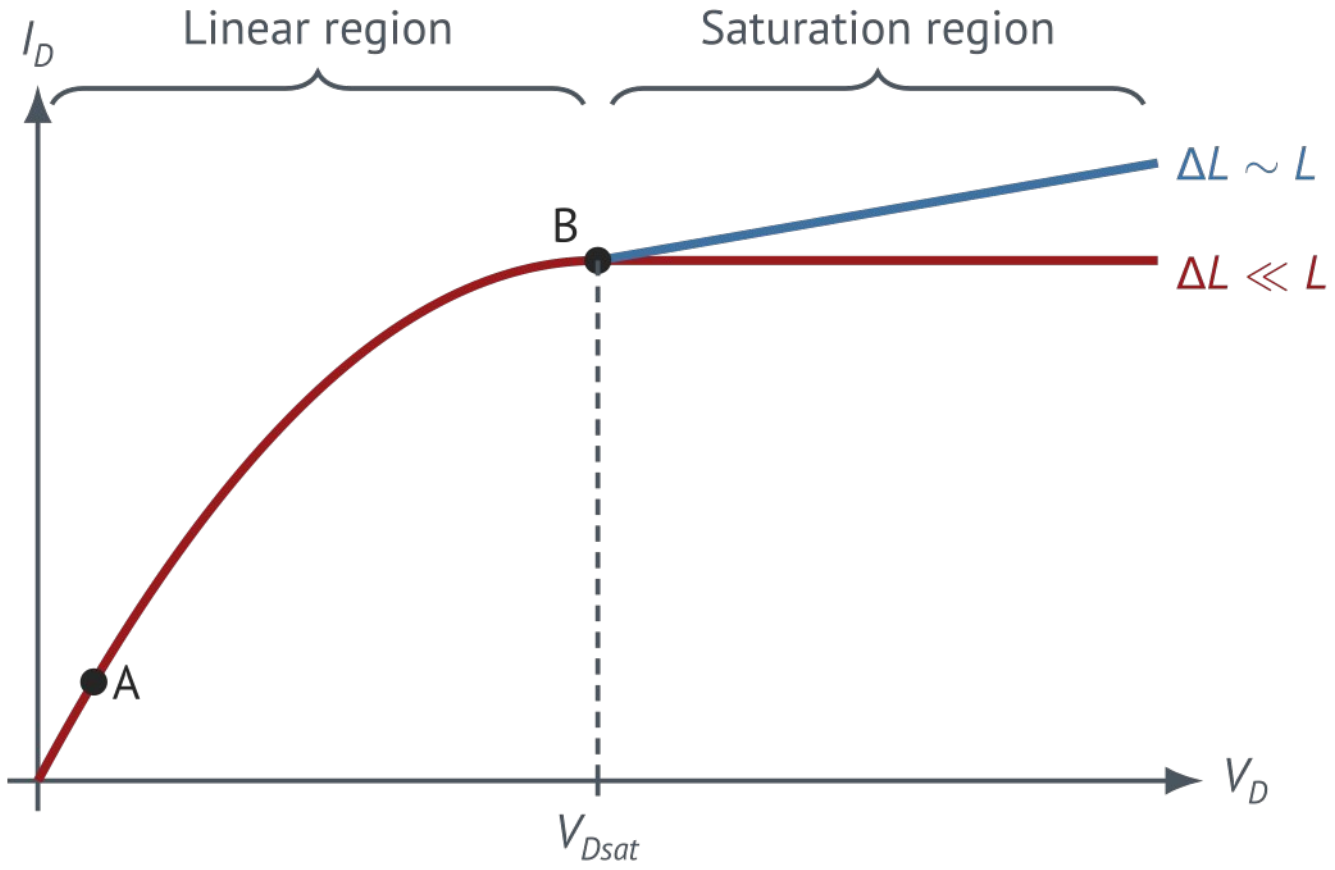
Pinch-off





I_D-V_{DS} characteristics for n-MOSFET

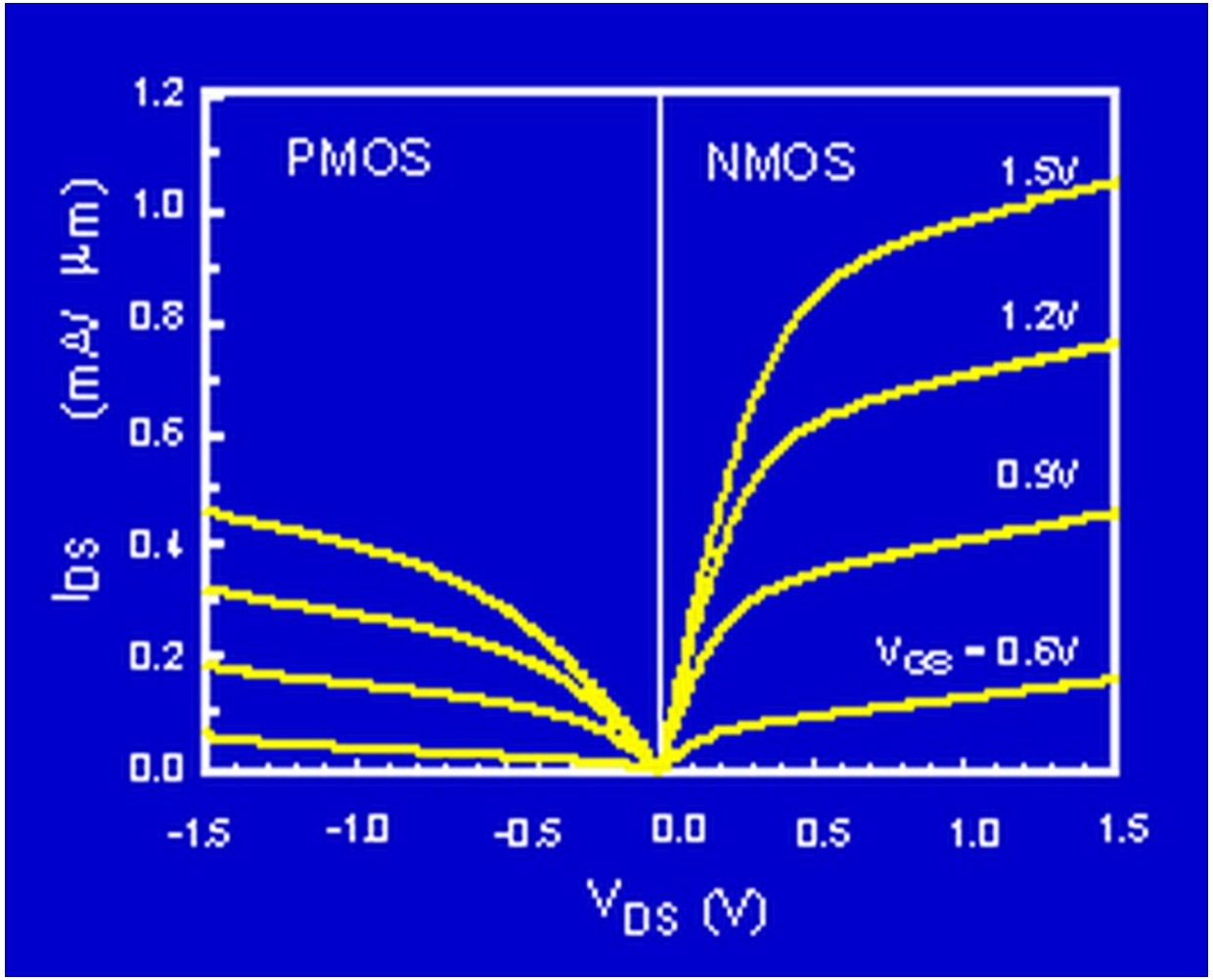
Linear region up to V_{Dsat}, then saturation: flat for a long channel, rising when ΔL is a large part of L.



- **A**: small V_{DS}; the channel acts as a resistor
- **B**: pinch-off at $V_{DS} = V_{Dsat}$
- **ΔL ≪ L** (long channel): the current stays flat
- **ΔL ~ L** (short channel): it keeps rising, channel-length modulation

P-MOSFET and N-MOSFET IV Characteristics

The PMOS curves mirror the NMOS curves, but at the same gate drive they carry about half the current.



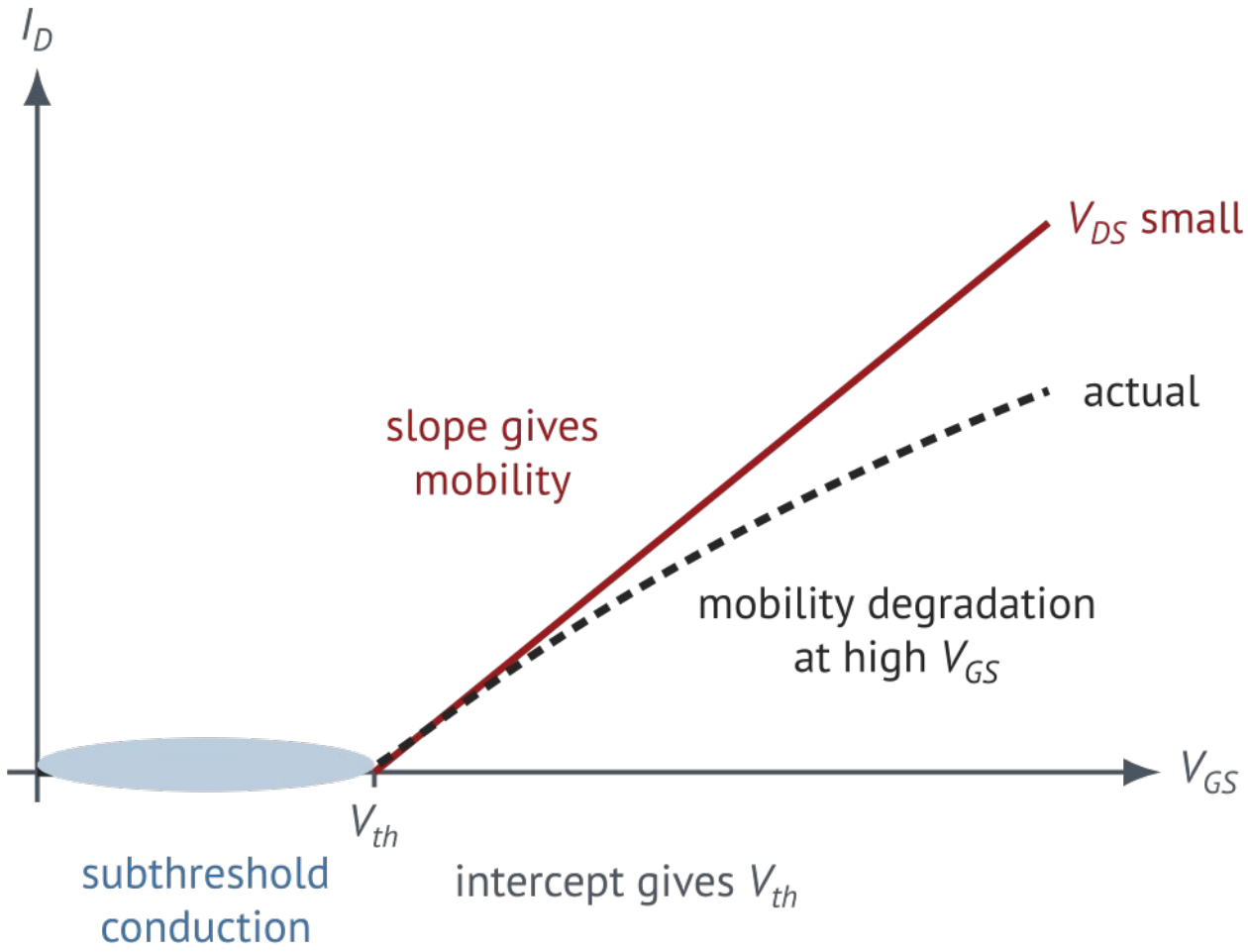
- PMOS: V_{DS} and V_{GS} negative; NMOS: positive
- Same shape: linear region, then saturation
- At the same $|V_{GS}|$, the PMOS current is **about half** as large

TRY IT

Why is the PMOS current about half as large?

Threshold and Subthreshold

At small V_{DS} the channel is a resistor: extrapolate the straight part to find V_{th}; its slope gives mobility.



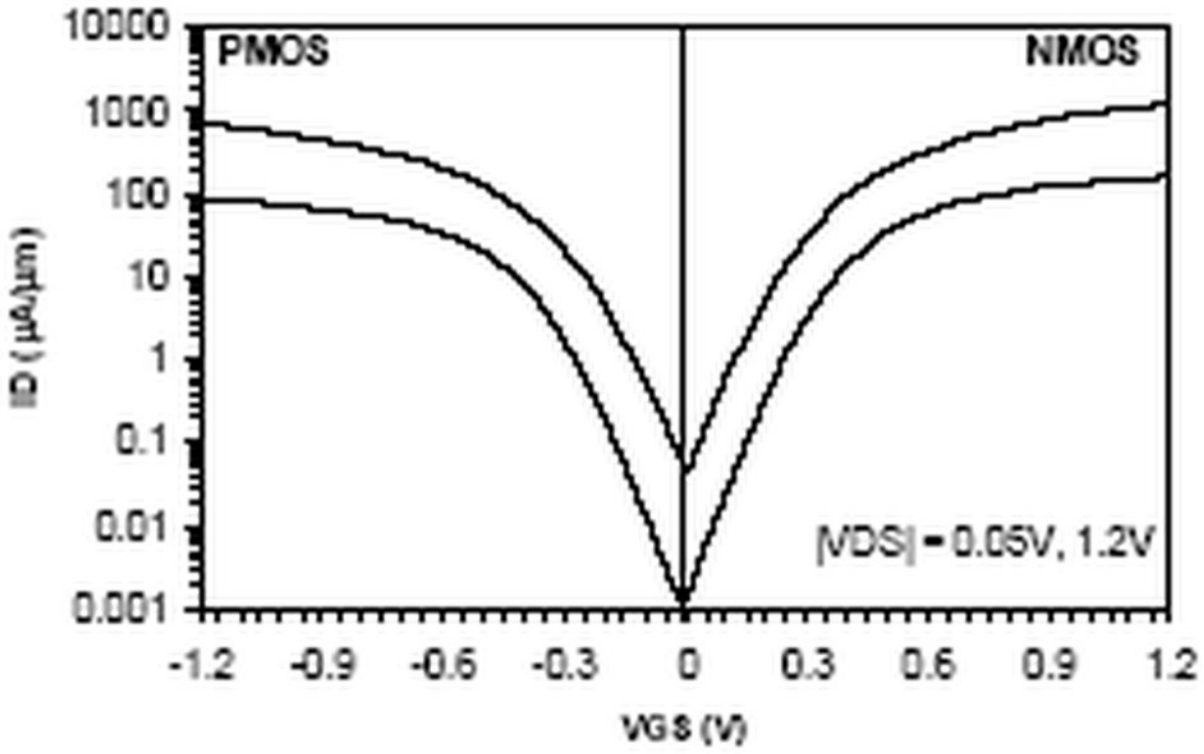
Linear region, small V_{DS}

$$I_D = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} = \frac{V_{DS}}{R_{CH}}$$

- Straight line: intercept $\mathbf{V_{th}}$, slope ∝ **mobility**
- Above: the actual curve bends down (mobility degradation)
- Below V_{th}: small, but not zero

Subthreshold Current

Below threshold the current is small, not zero: it falls exponentially, one decade per 65 to 90 mV.



Intel 90 nm technology, gate length 45 nm (NMOS) and 50 nm (PMOS); $|V_{DS}|$ = 0.05 V and 1.2 V. T. Ghani et al., IEDM 2003.

- The leakage that flows at $V_{GS} < V_{th}$ is the **subthreshold current**
- We assumed it was zero; in reality it is not
- The current at $V_{GS} = 0$ and $V_{DS} = V_{DD}$ is called $\mathbf{I}_{off}$

Subthreshold ($V_{GS} < V_{th}$)

$$I_D \approx I_0 \, e^{(V_{GS}-V_{th})/nV_T}$$